BIPOLAR JUNCTION TRANSISTOR

Bipolar Junction Transistor (qualitative background)
Two semiconductor PN junctions assembled back-to-back are used to form a transistor. However this is not simply a matter of connecting two diodes. It is essential that the junctions be formed in the same crystal so that the atomic background forces encompassing both junctions are continuous. Moreover for effective operation it is essential that the width of the region separating the two junctions be quite small.

There are two orientations in which back-to-back junctions can be assembled; in one case (NPN) the junctions share a common P region, and in the other case (PNP) they share a common N region. This common region is the ‘base’ of the device, and its doping uniquely characterizes the transistor type. The character of the transistor phenomena is formally the same for both orientations; the distinction between the two lies with details of the charge carrier transport.

In normal operation one junction, the emitter junction, is forward-biased and is used to inject charge carriers primarily into the central (base) region. The junction properties are optimized (and the junction specifically identified as the emitter) by the device manufacturer to perform this injection function. Ordinarily the two junctions would operate effectively independent of one another. However if the base width is made sufficiently (very) narrow the electrons injected at the emitter reach the second so-called ‘collector’ junction (also optimized and identified by the manufacturer as the collector). This junction is operated normally in reverse-bias so that the intrinsic collector junction current is just the very small reverse-bias current. However the collector junction does not distinguish between electrons present from one source or another, and the injected electrons transported across the narrow base become part of the overall reverse-bias current.

What makes this arrangement of particular interest is that the emitter junction current can be varied over a large range with small changes of emitter junction voltage. This is the usual forward-biased junction behavior. Since the carriers injected at the emitter virtually all reach the collector junction (the base width is made very narrow to assure this) the collector current is essentially just the emitter current (neglecting a comparatively small intrinsic leakage current). This augmented reverse-bias current is not sensitive to the collector voltage provided that collector junction remains reverse-biased. The transistor behaves closely as a controlled current source with a sensitive dependence on emitter junction voltage.

The icon used to represent a NPN transistor is shown below. The names have a historical origin in experiments that led to the development of the device. As indicated in the figure the emitter is identified readily as the only lead with an arrow. The emitter arrow always points in the direction of easy current flow for the junction, from the base out in the case of the NPN device, and into the base for a PNP device.

A plot of the collector characteristics (collector current IC vs. collector-base voltage, with emitter current IE as a parameter) for a representative NPN transistor (2N3904) is drawn below. (Note that the polarities are defined so that VCB ≥ 0 for reverse-bias of the collector junction.) The curve for IE = 0 corresponds to the intrinsic diode characteristic of the collector diode. The other characteristics essentially are displacements of the I_e = 0 characteristic, i.e., virtually all of the injected current simply adds to the intrinsic collector junction current. The current displacement increment is slightly smaller than the emitter current increment;
there is a small loss of injected carriers as they cross the base. However the loss is quite unlikely to be even as large as 5% and more than likely will be closer to 1% of the carrier flow.

![Graph showing collector characteristics](image)

In the normal operating mode (first quadrant; emitter junction forward-biased, collector junction reverse-biased) the characterization of the transistor as a current-controlled current source is clearly appropriate. Actually the collector junction can be slightly forward-biased before current is injected by the collector back into the base; a junction has a very small forward current for a forward bias below a ‘knee’ voltage of roughly 0.6 volt or so (for silicon).

**Ebers-Moll Model**

A well established first-order representation of the BJT (Ebers-Moll model) assumes first independent operation of two ‘back-to-back’ junctions, one to provide the carrier injection mechanism and the other to provide the carrier collection mechanism. To this is added a controlled current source to account for the ‘transistor action’, i.e., the mechanism by which carriers injected into the base through a forward-biased emitter junction almost all reach and pass through the reverse-biased collector junction to add to the collector current. This mechanism is what distinguishes a transistor from a simple back-to-back diode connection.

The circuit drawing to the right models the Ebers-Moll BJT representation. (Strictly speaking there should be a current source across the emitter junction reflecting possible ‘reverse’ operation, i.e., using the designated emitter junction as a collector and vice versa. Since the collector junction is a poor emitter and the emitter junction is a poor collector this reverse operation is rarely if ever used, and reflecting this disuse the emitter current source simply is omitted for simplicity.)

To illustrate the effectiveness of the E-M model a computer computation, plotted below, was made using nonlinear diode models and a typical value for $\alpha$ of 0.99. Compare this plot with the 2N3904 characteristics computed earlier.
Idealized Diode Model

For computational simplicity idealized diode models may be used rather than nonlinear diode models. Such use is convenient for hand calculations, particularly where preliminary design calculations are involved. A commonly used model is drawn to the right. The collector junction is modeled simply as an idealized diode. The emitter junction model uses a voltage source in series with an idealized diode, so taking into account in a simplified manner the threshold voltage for a forward-biased junction. A plot of the collector characteristics for the idealized diode model is shown below assuming $V_{BE} = 0.7v$ and $\alpha = 0.99$. Compare this with the characteristics computed earlier.

Idealized Diode CE BJT Model

For many if not most basic hand calculations an idealized diode simplification of the Ebers-Moll model makes important analytical insight into BJT circuit performance accessible with simplified calculations. For that reason it is worthwhile reviewing and expanding on the previous discussion of the Ebers-Moll model.

The basic Ebers-Moll model (NPN version) as introduced above is reproduced in the figure below, left. The diode icons are filled to indicate that the exponential diode characteristic is implied. The internal physics of the transistor make the expression of the collector current in terms of the emitter current a natural one. However in terms of circuit use it turns out to be generally convenient to replace the emitter current by the base current as a descriptor of the transistor characteristics. This is technically a matter of choice since Kirchoff’s Current Law requires $I_E = I_C + I_B$. The redefinition is made in the second part of the figure, and to emphasize the change the circuit is redrawn interchanging the orientations of the base and emitter in the drawing. Again this is a matter of presentation, without electrical consequence. Note particularly the re-expression of the controlled source current in terms of $I_B$. 
The final simplification is to use idealized diode models in place of the 'exponential' diodes. The emitter diode replacement also includes recognition of the nominal forward bias voltage of the emitter junction, although this is ordinarily omitted for the collector junction. The final idealized diode model is shown on the right.

It is worth emphasizing that the model change is one of convenience; exactly the same transistor properties are involved. It is only the manner of their presentation that is revised.

**BJT Example # 1**

A 2N3904 transistor is connected as shown in the diagram below (left). A source supplies $V_{CC}$ joules of work-doing ability to each coulomb of charge flowing through $R_C$ and the collector-base junction of the transistor. Part of this energy is expended in $R_C$ and part in the junction. The work done in $R_C$ depends on the collector current flowing, and this is controlled through the emitter source $V_E$.

This circuit shown is to be analyzed to determine the transfer characteristic $V_C$ vs $V_E$, given $R_E = 1\, \text{k}\Omega$, $R_C = 4.7\, \text{k}\Omega$, and $V_{CC} = 10\, \text{v}$. Assume (per manufacturer's device specifications) that $\alpha = 0.99$ and $V_{BE} \approx 0.7\, \text{v}$. We first perform an analysis using the idealized-diode model, and then compare conclusions from this analysis with a computer analysis using a non-linear transistor model. The conversion from the circuit diagram to use of the idealized diode model is illustrated above (right). It involves merely replacing the icon representing the real (nonlinear) device by the idealized -diode model (enclosed in the dashed rectangle). The problem now is the analysis of the two-diode circuit. There are in general four combinations of diode states to consider.

Consider, for example the case where the emitter junction is reverse-biased, so that $I_E = 0$; the circuit for this case is drawn to the right. The collector junction necessarily will be reverse-biased (since $V_{CC} = 10\, \text{v} > 0$), and so $I_C = \alpha I_E = 0$. Hence the voltage drop across $R_C$ is zero and so $V_C = V_{CC} = 10\, \text{v}$. (Incidentally note that the case where the emitter junction is reverse-biased and the collector junction is forward biased has been considered indirectly; it simply can't occur here.) In order that the emitter junction be reverse-biased require $V_E \geq -0.7\, \text{v}$. This is the 'cutoff' condition in which the emitter junction is not injecting current into the base at all.
As VE is decreased to become less than -0.7v the assumption of a reverse-biased emitter junction becomes invalid, and the emitter junction will become forward biased. The collector junction will remain reverse-biased. After all there would be no sudden discontinuity as the emitter junction changes state.

This circuit diagram for this case is illustrated to the left. A base-emitter loop equation determines

\[ I_E = \frac{(-V_{BE} - V_E)}{R_E} \]

Note that since we have required \( V_E \leq -V_{BE} \) for the emitter junction to be forward-biased, \( I_E \geq 0 \). With the collector junction reverse-biased

\[ V_C = V_{CC} - \alpha I_E = V_{CC} - \frac{\alpha R_C(-V_{BE} - V_E)}{R_E}. \]

or

\[ V_C = 10 - (0.99)(4.7)(-0.7 - V_E) \]

Operation with the emitter junction forward-biased and the collector junction reverse-bias is the 'normal', i.e., usual, operating condition of the transistor.

As \( V_E \) is made more negative the emitter current, and so the collector current, increases. Consequently the voltage drop across \( R_C \) increases, and so \( V_C \) decreases. All this is implicit in the expression for \( V_C \) as a function of \( V_E \). Eventually \( V_C = 0 \); this occurs when \( V_E = -2.85v \). And when this occurs the assumption that the collector junction is reverse-biased becomes invalid. Again the alternative is clear; operation changes to the 'saturation' mode, where both the emitter junction and the collector junction are forward-biased. In this circumstance the collector voltage is held to zero.

The circuit was analyzed by computer, using a nonlinear device model for a 2N3904 transistor. In addition the equation for \( V_C \) applicable for normal operation was plotted. The computed cutoff collector voltage of 10v occurs at about 0.6v (the corner is 'rounded corresponding to a real diode threshold voltage). Similarly the calculated estimate of the onset of saturation is -2.85v can be compared to the computed value.

This circuit operates (in the normal operating range) as a voltage amplifier, i.e., a change in emitter current is passed almost entirely to the collector. Since the emitter junction forward-bias voltage does not vary much for large current changes the change in emitter current is approximately \( \Delta V_E/R_E \). This is essentially the change in collector current (\( \alpha \approx 1 \)), and the change in collector voltage is \( (\Delta V_E/R_E)R_C \). The voltage 'gain' is a factor of \( R_C/R_E = 4.7 \) for the circuit analyzed.
BJT Example # 2

The amplifier circuit considered above is described as a 'Common Base' amplifier; the terminology indicates the transistor base is common to the input- and output terminal pair. A transistor amplifier assembled as drawn below, left, is described as a 'Common Emitter' amplifier. Use the idealized diode transistor model with base current as the control variable to calculate VC as a function of VB. Note that the modified model represents a convenient change in the description of the transistor model behavior, and not a change in the model behavior. Exactly the same prediction of behavior would be made using the same model as for the preceding illustration, with the following changes in the presentation: replace IE by IB + IC (KCL), and replace β by \( \frac{\alpha}{1-\alpha} \). However general experience has indicated the CE model to be the more convenient one to use in most circumstances.

The conversion from the 'real' transistor is made as shown below; one simply connects the model terminals to the appropriate circuit terminals. The analysis procedure is formally the same; for each combination of diode states determine the range of input conditions for which the assumed diode states are valid. There are four combinations of diode states, but as before the case where the emitter junction is reverse-biased and the collector junction is forward-biased can't occur (apply the same reasoning as for the preceding example.)

If the both junctions are reverse-biased KCL indicates IB = IC = 0, and so VC = VCC = 10v. This is the cutoff condition for the transistor. For the assumed emitter diode state to be valid it is necessary that VB \( \geq \) VBE. When VB crosses this threshold the emitter junction must become forward-biased (what else?) and the base current is

\[
IB = \frac{VB - VBE}{RB}
\]

We can anticipate the collector junction remains reverse-biased as the turn-on threshold is crossed; there is no sudden discontinuity in current or voltage. The collector current is \( \beta IB \), and so

\[
VC = VCC - \beta RC(VB - VBE)/RB
\]

or

\[
VC = 10 - 12(VB - 0.7)
\]

As VB increases the collector current increases, and VC decreases. Eventually VC = VBE, and the voltage across the collector junction is zero; the junction becomes forward biased and VC = VBE = 0.7v. This occurs for VB = 1.475v.

The circuit configurations for the three cases are drawn to the right with summary descriptions of circuit currents and voltages.

As for the preceding illustration the circuit was analyzed by computer, with the computed
results plotted for comparison to calculated estimates. (One estimate used $V_{BE} = 0.7v$, and a second used $V_{BE} = 0.6v$.

This circuit is a more effective voltage amplifier than that for the previous illustration because, assuming normal operation mode a small base current change produces a much larger collector current change (by a factor of $\beta$). The voltage gain here is calculated (estimated) to be 12; compare with the result of the computer analysis.

**BJT Example # 3**
The simple circuit drawn to the right actually occurs frequently in practice in one way or another. Consider $V_B$ and $R_B$ to correspond to the Thevenin equivalent of a signal source, and $R_E$ to be a load to which the signal is to be transferred. Almost inevitably, or so it seems, $R_E \ll R_B$ and so the voltage across $R_E$ is a small fraction of the voltage $V_B$ available from the source. While it might seem that the appropriate reaction is to increase $R_E$ this generally can't be done easily because of other constraints imposed on the load. It is possible however to 'trick' the source into believing it sees a high load resistance and concurrently to trick the load into seeing a low source resistance.

The transistor circuit shown is called an 'emitter follower', because as will be seen the emitter voltage change in normal operation is just a bit less than the base voltage change. We consider just normal operation here; in normal operation the emitter junction is forward-biased and the collector junction is reverse biased. The collector junction condition is satisfied for $V_{CC} \geq V_{BE}$; $V_{CC}$ will be a few volts typically and $V_{BE}$ is of the order of 0.7v. The condition for validity of the emitter junction assumption is simply $V_B \geq V_{BE}$.

The base current (see circuit diagram to the right) is calculated by writing a KVL equation around the base-emitter loop:

$$V_B = IB \cdot R_B + (\beta+1)IB \cdot R_E + V_{BE}$$

and since $V_E = (\beta+1)IB \cdot R_E$ calculate

$$V_E = \frac{V_B - V_{BE}}{1 + \frac{1}{\beta+1} \frac{R_B}{R_E}}$$

Note that $V_E \geq 0$ since the diode state assumptions require operation with $V_B \geq V_{BE}$.
Provided the circuit is designed with \( \frac{R_B}{(\beta+1)R_E} \ll 1 \) changes in \( V_B \) result in nearly equal changes in \( V_E \). But the emitter current is a factor of \( \beta + 1 \) times greater than the base current. For a given change in \( V_E \) the source provides considerably less current (and so effectively 'sees' a higher resistance) than flows in the emitter. The higher emitter current is the consequence of the transistor action represented by the controlled current source.

This analysis illustrates an important benefit of using the idealized-diode model. Computer programs and highly sophisticated device models make numerical analysis of circuits relatively simple to perform. However it is at best difficult to conclude from a numerical analysis that the desired circuit operation depends on the condition \( \frac{R_B}{(\beta+1)R_E} \ll 1 \); knowing this it is much simpler to specify (design) circuit element values to meet the requirements of a specific application. Fine tuning of the circuit design then can be done with computer assistance.

**BJT Example # 4 (PNP Transistor)**

The PNP transistor is formed by two closely spaced junctions similarly to the NPN device, but with a common P region. Physical phenomena, descriptive equations, etc formally are the same as for the NPN transistor. The critical circuit difference to take note of involves the junction polarities. For example forward-bias of the emitter junction of a PNP transistor means it is the emitter that is positive relative to the base. Similarly to reverse-bias the collector junction of a PNP transistor the collector is negative relative to the base.

The nominal junction ('knee') voltage difference for forward-bias is the same in both cases but whereas for the NPN transistor the base is positive relative to the emitter the geometry difference means the emitter is positive relative to the base for the PNP transistor.

The PNP icon and the idealized diode equivalent circuit are shown in the following figure. Note the reversal of the diodes from that of the NPN case. It is often convenient to reverse the polarity arrow for both \( I_B \) and for the controlled current source, although this is only a cosmetic change (what is technically important is the relative polarity).

Consider the voltage amplifier circuit shown in the figure below. The PNP transistor is oriented with the emitter on top. This does not affect the device characteristics of course, but it enables use of a positive voltage supply \( V_{EE} > 0 \) to bias the circuit. For the present analysis we suppose normal operation, i.e., emitter junction forward-biased and collector junction reverse-biased. To assure the emitter junction condition requires

\[
V_{EE} - V_{BE} \geq V_B.
\]

(Note the polarity of \( V_{BE} \); this voltage corresponds to the emitter junction threshold voltage in forward bias).

Calculate \( I_B = (V_{EE} - V_{BE} - V_B)R_B; \) \( I_B \geq 0 \) because of the requirement for normal mode operation. (Incidentally a transistor doesn't automatically operate in normal mode. Circuit parameters must be specified to make it so explicitly.) The collector current then is \((\beta+1)I_B\), and \( V_C \) is \((\beta+1)I_BR_C\).

**BJT Example # 5**

The transistor is not exactly a precision device; manufacturing tolerances, temperature sensitivity, and second-order effects conspire to make parameters such as \( \beta \) uncertain by a factor of two or more. Nevertheless with appropriate care it is possible to design for relatively precise operation. This last example illustrates this. The circuit is the same as the NPN voltage amplifier considered before, except for the
addition of the emitter resistor $R_E$. Once again we limit the discussion to normal operation, with the equivalent circuit as shown below.

It is left as an exercise to calculate

$$I_C = \frac{\beta}{\beta + 1} \frac{V_B - V_{BE}}{R_E + \frac{R_B}{\beta + 1}}$$

(Write a loop equation around the base-emitter loop, noting that the emitter current is $I_E + \beta I_E$.)

The transistor properties enter into this expression in the parameter $\beta$ and in $V_{BE}$. The factor $\beta/(\beta+1)$ is approximately 1 (for $\beta = 99$, for example, it is 0.99) and in any event the ratio varies little. Provided we select resistor values which make $R_E \gg R_B/(\beta+1)$ the influence of any variation in this term on the collector current will be greatly reduced. Finally the variation in $V_{BE}$ turns out to be of the order of 0.2 volts over a 100°C temperature range. By making $V_B \gg 0.2$ volts the effect of this variation is reduced. Note that it is not necessarily a straightforward matter to select circuit values to effect the constraints in all circumstances. On the other hand it is easier to do the selection guided by the approximate results of the idealized diode analysis, and subsequently refine the selections using a computer assisted analysis.

**Amplification using a BJT**

The transistor circuit in the following figure includes the basic elements of a transistor amplifier. It is, of course, possible to enhance amplifier performance considerably using sophisticated modifications and additions to this circuit. However the immediate purpose here is not to describe a high-performance amplifier, but rather to discuss the essential principles of amplifier operation.

First it useful to recognize that there is no ‘universal’ amplifier that does everything well. Invariably optimizing performance in one respect degrades performance in a different respect. For the present purpose we examine an amplifier intended to accept a small time-varying voltage as input, and produce an amplified copy of that voltage as output. The energy efficiency of such an amplifier is typically terrible. Nevertheless the inefficiency is acceptable because the amplifier ordinarily is operated at relatively low power levels. Designing an efficient power amplifier is an important special topic in its own right.

The next figure provides a sort of map for the discussion following.
for certain uncommon applications a voltage source is preferred to a current source. A voltage source in a stand-by condition dissipates no energy, since there is no current flow. (More realistically, it dissipates a minimal stand-by power.) A current source by definition must maintain a current flow even in a stand-by condition, with inevitable significant losses. A DC source is used (again with rare exception) to avoid any interaction between time variations of an AC energy source and the time variations of the signal to be amplified.

Each coulomb of charge transferred through the source is provided a work-doing ability of VCC joules. This is the circuit energy (per coulomb) available to do work in supporting the amplification process. The source power is VCC (joules/coulomb) times the source (collector) current (coulombs/second).

**BJT**

The transistor is the circuit control element with which the energy flow provided by the voltage source is regulated in proportion to an input signal. Note that the transistor model functions essentially as a current-controlled current source. For amplification applications the transistor would normally operate in normal mode, i.e. with the emitter junction forward-biased and the collector junction reverse-biased. It does not do this automatically of course; the circuit must be designed specifically to support the desired operation.

**Biasing**

A basic consideration in amplifier design is setting the quiescent operating state of the transistor, i.e., establishing the collector current and collector-emitter voltage in the absence of a signal to be amplified. Where to set this quiescent operating point depends in general on specific circumstances of the application. However the means of doing so are to a large extent the same whatever the specific application.

The base current (see the circuit above) is determined by writing a KVL equation around the base-emitter loop. Thus VBB = IB RB + VBE. The transistor base-emitter junction voltage is substantially constant whatever the base current, since the junction current is exponentially dependent on the junction voltage. A representative value often used for silicon devices is about 0.7V. However there may be a an uncertainty in this value as large as about 0.2V, representing variations associated with manufacturing tolerances and temperature dependence. Ordinarily a circuit design would choose VBB > 0.7V to limit the influence of the uncertain value of VBE. The collector current then would be estimated with some assurance to be ßIB.

After the collector current is established the collector resistor RC is used to set the quiescent collector voltage; VC = VCC – IC RC. Note that setting the DC collector voltage involves dissipating energy in RC. This dissipation can be (and often is) substantial. For example suppose VC is to be set to VCC/2 (approximately) to allow equally for collector voltage changes above and below the quiescent Q value. The voltage source then supplies a power VCC IC, and the collector resistor alone dissipates half this power. (A major part of the remaining power is dissipated in the transistor, even when a signal is being amplified.)

It is uncommon to design a BJT circuit graphically, because the device parameters have large manufacturing tolerances and significant temperature sensitivity. Idealized models (and subsequent computer assisted fine tuning) serve much better. Nevertheless it is useful pedagogically to visualize circuit operation graphically. Thus, in the figure to the right, consider the set of collector characteristics shown. The steady state operating point of the circuit (VC, IC) must be a point on one of these characteristics. In particular it must lie on that particular characteristic corresponding to the base current IBQ = (VBB–VBE)/RB.

In addition KVL and Ohm’s Law require VC = VCC – IC RC. This is the equation of a line which, plotted on the IC, VC coordinate plane, has a intercept on the ordinate of VCC/RC and an intercept on the abscissa of VCC (see figure). The operating point (Q point) is required to be somewhere along this line. In particular, to satisfy both requirements, it must be the intersection of this line with the IBQ transistor characteristic.
Amplification
Suppose the base voltage is changed, say increased by a small amount $\Delta V$ (small enough however that the transistor remains in normal active operation). There will be a corresponding increase in $I_B$, and so also an increase in $I_C$; $\Delta I_C = \beta \Delta V/R_B$. Corresponding to this there is a decrease in collector voltage of $-R_C(\beta \Delta V/R_B)$. The corresponding voltage gain is $-\beta R_C/R_B$. (The physical interpretation of this is that a base voltage change produces a base current change inversely proportional to $R_B$. Then, reflecting the transistor action, this current change is multiplied by $\beta$ to form the collector current change, and the collector current change produces a voltage change across $R_C$. Note the large electrical current ‘lever’ provided by the transistor current gain.)

Epilogue (Sort of)
BJT Example #2 discussed above is an illustration of the simplified amplifier circuit described. The derivation there shows that an incremental change in the base voltage produces an incremental change in the collector voltage magnitude twelve times greater.

The amplifier as described actually is not well designed, and indeed it is not. Indeed it is likely to function poorly if at all because of various manufacturing and environmental uncertainties. It is used simply to describe fundamental aspects of amplifier operation.
**Problem 1**

Estimate, using the idealized-diode transistor model, the collector current for each transistor in the diode-connected transistor biasing circuit shown. Assume Q1 and Q2 are identical devices with $\beta=120$.

**Answer**

The idealized-diode equivalent circuit is drawn below. Note that Q1 operates as a transistor; the collector-base junction is not forward-biased. Clearly the Q1 emitter junction will be forward-biased. The current through the 10kΩ resistor is $\approx (10 - 0.7)/10 = 9.3\text{ma}$.

While not necessary the analysis may be simplified by taking advantage of the fact that the solution for a linear circuit is unique. Thus we can make some not unreasonable approximations, analyze the circuit based on the approximations, and then verify that the approximations are consistent with the analysis.

Thus assume, subject to verification, that the Q2 base current is negligible compared to the Q1 collector current. Q1 and Q2 will carry more or less the same emitter current since they are identical devices with the same emitter junction voltage. Since the transistor $\beta$ is large the current assumption is not unreasonable. In fact for a Q2 emitter current of 9.3 ma the Q2 base current would be $9.3/120 = 0.078\text{ ma} << 9.3\text{ ma}$.

The results of a computer computation of the circuit currents, using non-linear transistor models is drawn below. The plot compares the Q1 and Q2 collector currents over a wide temperature range. (Note the scale for the current.) There is roughly a 20µa variation in current, about a 2% absolute change. The small difference ($= 60\mu\text{a}$) in the two collector currents actually is because of a small second-order increase of collector current with collector voltage; the Q2 collector voltage is higher than that for Q1.
Problem 2)
Given the circuit shown: estimate the collector current. Use the idealized-diode transistor model analysis with \( V_{BE} = 0.7\text{v} \) and \( \beta = 120 \), and verify that

\[
I_E = \frac{V_{BB} - V_{BE}}{R_E + \frac{R_B}{\beta + 1}}
\]

Answer
Recall that the collector current will change an order of magnitude for roughly a 50mv change in junction voltage, two orders of magnitude for a 0.1volt change. Since the base supply voltage is 4 volts an uncertainty in \( V_{BE} \) of even as much as 0.4volt results in only a 10% change in the value of the numerator. Hence using the nominal value will not greatly affect the current estimate. Similarly with a minimum \( \beta \) of 99 the second term in the denominator is 0.15 K\( \Omega \) compared to the first term value of 3.3 K\( \Omega \). Ignoring the second term entirely changes the denominator by less than 5%. Hence using the nominal value for \( \beta \) will not greatly affect the current estimate. The emitter current estimate of 0.96 ma is largely independent of the transistor parameters \( V_{BE} \) and \( \beta \). A computer computation of the collector current over a 100˚C temperature range, using a nonlinear 2N3904 transistor model, is plotted below. (Note the scale for the current.)

![Collector Current vs Temperature Graph](image)

Problem 3)
Using the idealized-diode transistor model estimate the collector current in the PNP bias circuit shown. Nominal transistor parameters are \( V_{BE} = 0.7\text{v}, \beta = 120 \).

Answer
Replace the BJT by the simplified PWL model as shown on the left. Note that the biasing arrangement reduces the influence of the BJT parameters in establishing the current value, and so 'typical values' from manufacturer's specifications may be used with some confidence.

Replace the biasing resistors by their Thevenin equivalent \( 33K\|82K = 23.5K \), and the Thevenin voltage \( (82/(82+33))10 = 7.13\text{v} \) to obtain the equivalent circuit as shown. Avoid the not uncommon careless topological error of confusing the PNP transistor with a NPN transistor.

Write a base-emitter loop equation as was done for the NPN configuration discussed above; again avoid the topological error confusing the emitter and collector. Solve for \( IC = 120IB = 0.91\text{ ma} \). A computer analysis provides the collector current 0.935 ma.
Problem 4
Assume (subject to subsequent verification) that the Q2 base current can be neglected compared to the Q1 emitter current. (Why so?) Calculate the voltage at the collector of Q2. Assume 2N3904 devices (VBE = 0.7v, β = 120).

Answer
The voltage across the 220Ω is less than that across the 680Ω, and hence anticipate the two emitter currents are roughly in proportion to the resistors. With a β > 100 the base currents will be an order of magnitude or more greater than the emitter currents.

Neglecting the Q2 base current (compared to the Q1 emitter current) allows the Q1 biasing to be treated independently of Q2. Hence

\[ I_{E(Q2)} \approx \frac{0.68 I_{E(Q1)} - 0.7}{22} = 9.79 \text{ ma} \]

Determine \( I_{E(Q2)} \) from the Q1 emitter voltage.

To substantiate the approximation used verify that the Q2 base current, \( \approx \frac{5.13}{121} = 0.04 \text{ ma} \), is small compared to the Q1 emitter current of 4.2 ma. For comparison a computer computation provides \( I_{E(Q1)} = 4.3 \text{ ma and } I_{E(Q2)} = 9.98 \text{ ma} \).

Problem 5
Calculate the emitter current in the circuit shown. Comment: Circuit analyzers who do not verify assumptions they make are often surprised.

Answer
Assume, subject to verification, that the transistor is biased in normal forward mode, i.e., emitter forward-biased and collector reverse-biased. Replace the base biasing resistors by a Thevenin equivalent voltage source of \( 9 \frac{3.3}{3.3+6.8} = 2.94 \text{v} \), in series with a resistance of \( \frac{3.3 \cdot 6.8}{121} = 2.22 \text{KΩ} \). Use a nominal β of 120 and a VBE of 0.7v to estimate the emitter current as \( \frac{2.94-0.7}{1+(2.22/121)} = 2.2 \text{ ma} \).

But since the collector current is essentially equal to the emitter current the voltage drop across the 5.6KΩ collector resistance would be 12.3v, making the collector voltage negative! The assumed reverse-biased state of the collector diode is inconsistent, and the calculation is invalid. The actual collector junction state is actually forward-biased, i.e., the transistor must be operating saturated. The PWL model in this case is as shown to the right (both diodes ON). Solve (for example) for the node voltage \( V = 2.2 \text{v} \), and so the emitter current is 1.5 ma, and the collector current is 1.2 ma. A computer analysis computes a collector current of 1.3 ma, and an emitter current of 1.6 ma.

Problem 6
Determine the Q2 collector voltage for the complementary pair' biasing configuration shown. Assume 2N3904 and 2N3906 devices VBE = 0.7v, β = 120. Hint: Assume subject to subsequent justification that the Q2 base current can be neglected compared to the Q1 collector current.

Answer
The Q2 base current is likely to be negligible compared to the Q1 collector current (an assumption to be verified), and if this...
approximation is applied calculation of the Q1 biasing is independent of Q2. Estimate that the Q1 emitter current is 1.15mA. The Q1 collector voltage then is 8.21v, and so the Q2 emitter current is estimated to be 2.0mA. These estimates are consistent with neglecting the base currents. Node voltages and device currents determined by computer analysis are:

- Q1 collector voltage = 8.1928
- Q2 collector voltage = 4.5061
- IC(Q1) = 1.16 mA
- IC(Q2) = 2.05 mA

**Problem 7**

Estimate the collector voltage of Q2. Use the idealized models and assume $\text{VBE} \approx 0.7\text{v}$ and $\beta = 120$.

Hint: Anticipate subject to subsequent justification that the Q2 base current may be neglected compared to the Q1 collector current. Then write a loop equation $\text{VCC} \rightarrow 3.3K \rightarrow \text{Q2 emitter} \rightarrow \text{Q1 base} \rightarrow \text{ground} \rightarrow \text{VCC}$; this involves only a single current variable.

**Answer**

Neglect the base current of Q2 relative to $I$, the collector current of Q1, and write the loop equation as described above:

$$9 = 3.3I + 0.7 + 47(I/120) + 0.7$$

to determine $I \approx 2.06\text{ ma}$. The estimate the Q1 collector voltage as $9 - (2.06)(3.3) = 2.2\text{ v}$. The Q2 emitter voltage then is $\approx 1.5\text{ v}$, and the Q2 emitter current is $1(1.5/1) + (1.5 - 0.7)/47 = 1.52\text{ma}$. A PSpice computation gives the collector current of Q1 as 2.1mA and the collector current of Q2 as 1.36mA.