Objective

Preferably (in general) electronic circuitry is energized from a voltage source, i.e., a source for which ideally no current flows under open-circuit conditions. Absent the need to maintain the load current stand-by power dissipation will be minimal. In addition a DC (unipolar constant voltage) power supply virtually always is preferable over an AC supply for electronic equipment. An AC supply couples power supply dynamics with circuit signal dynamics, whereas ordinarily a DC supply introduces no special time relationship.

However commercial electrical energy ordinarily is generated by rotating machinery and has a sinusoidal waveform; it is distributed as such from a primary generating station to substations, and ultimately to a consumer. An electronic ‘power supply’, as the term usually is interpreted, accepts a sinusoidal input voltage and converts it (ideally) to a constant DC output.

In this note introductory concepts used for making the conversion are examined in the context of a semiconductor diode rectifier. There are typically two steps to the conversion; a bi-directional (sinusoidal) AC input voltage is ‘rectified’ to form a unidirectional waveform, and this waveform is ‘filtered’ to provide a (nearly) constant magnitude.

Half-Wave Rectifier

Assume, for the moment, that the capacitor in the diode circuit diagram to the right is absent. One cycle of a sinusoidal source voltage is sketched to the left of the circuit; the positive half-cycle is filled simply to distinguish it clearly from the negative half-cycle. The diode conducts only in forward bias, i.e., only during the positive half cycle. Current flowing through the diode produces a voltage across the load resistance during this half-cycle. Since there is negligible conduction during the other half-cycle the load voltage during this period is zero. The waveform sketched to the right f the circuit illustrates this rectification.

By converting the bipolar waveform to a unipolar one a DC waveform is ‘approached’, at least in the sense that unlike the sinusoidal waveform the average value of the voltage over a cycle is greater than zero. It is however not a constant DC waveform, which is what is needed to avoid interactions with supply voltage timing.

One approach towards reducing the variation involves separating the processes of providing and distributing the energy. Thus the source is not used to supply the load energy directly but rather to deliver the energy to a reservoir during the conducting half-cycle; the reservoir then is designed to release the stored energy more or less uniformly over the full cycle.

This is the purpose of the capacitor, which has been ignored until now. During the positive half-cycle the power source is used primarily to charge the capacitor. During the negative half-cycle, when the diode blocks current flow from the source, the capacitor discharges, acting as a temporary energy supply for the load resistor. The capacitor functions (in a manner of speaking) as a rechargeable battery,
continually charged during one half-cycle and discharged during the other. That is the essential concept; the details are a bit more involved.

Suppose that the power supply has been operating long enough to reach a steady state, i.e., initial turn-on transients have become negligible. The steady-state condition (as will be verified) for one full cycle of the source frequency is as shown in the figure below. For convenience consider the circuit behavior starting from the time the diode begins conduction at $t_1$. The AC source resistance is generally small (to avoid wasting power) so that the capacitor charges fast enough to track the source waveform. Once past the peak value the source voltage amplitude decreases sinusoidally. However the capacitor charge cannot flow back through the diode and so the capacitor voltage must decay exponentially through the load resistor. It is not difficult to show that the sinusoid decreases faster than the exponential, so that at some time $t_2$ the diode becomes reverse-biased! At that point the source no longer supplies energy to the load; the load current is provided entirely by the capacitor discharge. Eventually of course the source begins the next positive half-cycle, and the diode is again forward-biased. This occurs one full cycle after $t_1$, and the waveform repeats.

A mathematical description of this process involves transcendental functions, and requires a numerical analysis to obtain precise design information. This is not difficult to do on a computer but for the purpose of establishing an initial trial design it is neither desirable nor necessary to explore the transcendental expressions to identify key parameters and obtain good approximations to several important design equations. Indeed some things are fairly clear. For example the exponential decay clearly involves the time constant $R_L C_L$. The larger this time constant the ‘flatter’ the exponential decay, and the closer the approximation to a constant waveform. The time constant $R_L C_L$ therefore should be ‘large’ compared to the sinusoidal period $2\pi/\omega$, i.e., $\omega R_L C_L >> 2\pi$.

How large should ‘large’ be? We can obtain a criterion for evaluating this issue in the following way. A large time constant implies a small conduction angle; the flatter the exponential decay the faster the sinusoid drops by comparison. Hence suppose we neglect the conduction angle (approximate it as zero), in anticipation of a ‘good’ design. Moreover, it is a small matter for preliminary estimates, neglect the small diode forward-bias voltage. Then the exponential starts its decay roughly at the peak of the sinusoid with amplitude $E(t=0)$. The load voltage during the time the diode is not conducting is $E_L(t) = E e^{-t/RC}$. The exponential decay ends at $t = 2\pi/(\omega R_L C_L)$, i.e. one cycle later (still approximating the conduction angle as zero). For good rectification, i.e., small exponential decay, note again that it is desirable to make $\omega R_L C_L >> 2\pi$. This implies a small value for the exponent in the exponential expression, and on this basis we may approximate the exponential to first order by the first two terms of a power series expansion. From this the ‘peak-to-peak ripple’ $V_r = E_L(0) - E_L(2\pi/(\omega R_L C_L))$ may be determined to be $2\pi E_L/\omega R_L C_L$; the ‘ripple’ is the difference between the maximum and minimum.
values of the load voltage, and so is a measure of the constancy of the voltage. Divide by $E_L$ to normalize to the peak amplitude. Note that $2\pi/\omega R_L C_L$, is the ratio of the period of the sinusoid to the time constant.

The conduction angle $\theta$ can be estimated (particularly for a ‘good’ rectifier) by noting that conduction occurs approximately from the point where the diode begins to conduct to the sinusoidal peak, i.e., at $\sin((\pi/2)-\theta) = \cos \theta = 1 - 2\pi/\omega R_L C_L$. Approximate $\cos \theta$ by the first two terms of its power series expansion, i.e., as $1-(\theta^2)/2$, and find $\theta^2 \approx 2\pi/\omega R_L C_L$. As was anticipated small conduction angle is associated with small ripple.

It is almost trite but nevertheless significant to recognize that when the diode conducts the voltage across the capacitor begins to change, and moreover that change is accompanied by a capacitor current ‘spike’. This capacitor current, an addition to a current component also provided during the conduction angle by the source, may be estimated by differentiating the supply voltage and evaluating it at the onset of conduction (maximum rate of change);

$$\text{capacitor current spike} = C_L \frac{d}{dt} \left( E_L \sin \theta \right) = \omega C_L E_L \cos \theta \approx \omega C_L E_L \left(1 - \frac{\theta^2}{2} \right)$$
$$\approx \omega C_L E_L \left(1 - \frac{V_t}{E_L} \right) \approx \omega C_L R_L \left( \frac{E_L - V_t}{E_L} \right)$$

The term in parentheses in the last form of the expression is, roughly, the load current. Since a ‘good’ design wants $\omega R_L C_L >> 1$ it follows that the capacitor current spike can be expected to be considerably larger than the load current, and rectifier diodes must be selected accordingly. Note that the spike as estimated is a recurrent phenomena, i.e., for each cycle. The current spike recharges the filter capacitor during a short conduction period. And the capacitor then provides energy to the load. In general however, there will be a larger start-up spike since the capacitor would likely be uncharged initially, and current will be limited primarily by the small internal resistance of the sinusoidal source.

**Illustrative Circuit**

The netlist for an illustrative computation is shown below, and following that the computed data is plotted. (The 1N4004 is a general-purpose diode for low-power rectification service.) A PSpice netlist for a half-wave rectifier circuit follows; note that the analysis is repeated for three values of the ‘filter’ capacitor.

```
*  HALF-WAVE RECTIFIER

VS 1 0 SIN(0 10 60 )
D1 1 2 D1N4004
RL 2 0 1K
CL 2 0 {CVAL}

.PARAM CVAL = 1U
.MODEL D1N4004 D(Is=14.11n N=1.984)
+ Rs=33.89m Ikf=94.81 Xti=3 Eg=1.11
+ Cjo=25.89p M=.44 Vj=.3245 Fc=.
+ Bv=600 Ibv=10u Tt=5.7u
.TRAN10U 40M 0 10U
.PROBE
.STEP PARAM CVAL LIST 1U 10U 50U
.END
```

Circuits  Diode Rectifiers  M H Miller:
Using the approximate relationship derived above the peak-to-peak ripple for a 50µF capacitor is estimated to be 3.3 volts, close to the computed value. (What happens if a 100µF capacitor is used?) Incidentally take note of the effect of the diode forward-bias voltage which causes a difference of a few tenths of a volt between the peak values of V(1) and V2). Note also that the 1N4004 is rated for a reverse-bias breakdown voltage of 600 volts, so operation is well within ratings.

The diode and load currents for the 50µF case are plotted next; note the convenient scaling of the load current (also emphasizing the magnitude of the current spike). For the 50µF capacitor the estimate for the conduction angle \( \theta \) is \( \sin \theta \approx 1 - .33 \), and \( \theta \approx 42^\circ \). Compare this estimate with the conduction angle read from the plotted data. For this filtering \( \omega R_L C_L = 18.85 \). The average load current then is estimated as \( (10 - 3.3)/1K = 6.7 \) ma the approximate expected current spike would be \( 18.8 \times 6.7 \approx 126 \) ma peak. Note that the startup spike is considerably larger, reflecting the faster rate of change of voltage because of an initially uncharged capacitor. Assuming the conduction angle typically would be (roughly) 30° the start-up spike here is twice the steady-state spike.

**Illustrative Problem: Half Wave Rectifier**

1) Design a half-wave diode (1N4004) rectifier circuit as discussed above to the following (nominal) specifications:
   - 12 V peak, 60 Hz supply voltage
   - 1 KΩ load resistance
   - P-P ripple < 1 volt
Answer
The ratio of the peak-peak ripple to the sinusoidal peak voltage is: \( \frac{\text{P-P ripple}}{V_p} \approx \frac{2\pi}{(\omega RC)} \)

The rectified voltage peak \( \approx 12 - 0.7 = 11.3 \text{ volt.} \)

P-P ripple \( \approx 11.3 \left( \frac{2\pi}{\omega RC} \right) \).

For P-P ripple < 1 estimate \( C > 188\mu\text{F} \) will suffice; use \( C = 200\mu\text{F} \).

The conduction angle is found from:
\( \theta^2 \approx \frac{4\pi}{\omega RC} = 0.17 \text{ for } C = 200\mu\text{F}, \text{ and } \theta = 0.41 \text{ radian (\approx 23º)} \)

The computed rectified output (netlist on the right) is plotted below showing the initial charging of the capacitor (from an initial uncharged condition).

The diode current pulse also is compared (below) with the load current. Note that the load current magnitude is multiplied (more or less arbitrarily chosen) by a factor of 50 for convenience. The load current is approximately 10ma, whereas the initial current spike is nearly one ampere.
**Full-Wave Bridge Rectifier**

In the half-wave rectifier circuit source power is provided from the source only during a small conduction angle near the peak of the positive half-cycle. Observe however that by reversing the diode orientation power would be supplied during the negative half-cycle rather than the positive half-cycle. This suggests powering the load using two half-wave rectifiers, one conducting only during the positive half-cycle and the other only during the negative half-cycle. It is necessary, of course, to assure that both rectifiers supply current that flows through the load in the same direction. A diode ‘bridge’ circuit to accomplish the desired end is drawn to the right.

As before temporarily ignore the capacitor. During the positive half-cycle, i.e., $V(1,3) \geq 0$, diodes $D_1$ and $D_2$ are forward-biased, and load current flows through $R_L$ from node 2 to node 0.

The other two diodes are reverse-biased, and so not active in the circuit. Effectively the circuit during the positive half-cycle is as shown in the diagram below, left. Except for using two diodes rather than one this is the half-wave rectifier configuration. For the negative half-cycle the circuit is effectively as shown below, right. Note that except for the source the circuit configuration although geometrically flipped vertically is electrically the same as before. The special consequence of this topological reversal is to cause the rectified current to flow though the load resistor in the same direction for both half-cycles, so that the source is connected during both half-cycles to provide unipolar load power.

Circuit operation then is as described before, except that the capacitor is recharged on both half-cycles. Hence the exponential decay for a given filter capacitor is essentially halved, improving the peak-to-peak ripple for a given capacitor value. The reason for using two diodes for each half-wave circuit should be clear at this point; it is necessary to prevent short-circuiting. A secondary consequence of this is that the load voltage amplitude is lowered from the source voltage by two diode drops.

It is interesting to note again that (for a small-ripple design) the source conducts only for a short fraction of each half-cycle. During the small conduction angle the capacitor is charged, and it is the discharge of the capacitor during the remainder of each half-cycle that provides the load current.

A bridge circuit characteristic of importance is that the load resistor and the source cannot have a common ground point; usually one end of the load is grounded as shown in the circuit diagram. Incidentally since a larger RC product promotes smaller ripple it follows that low-current (large load $R$) supplies have an advantage.
A computation for a bridge rectifier illustration (netlist below) follows. All diodes used are 1N4004, \( R_L = 1k\Omega \), and the source voltage is a 60Hz, 10 volt peak sinusoid. Three values for the filter capacitance are used (Note: \( C_L = 1\,\text{nF} \approx 0 \) capacitance effectively.)

This output plot is similar to that for the half-wave rectifier, except that the source voltage is not drawn. Compare with the half-wave rectifier plot, observing particularly the contribution of the negative half-cycle. As already noted the recharging process occurs during both half-cycles halving (approximately) the exponential decay time. All the estimation expressions apply here with the provision that the half-cycle period be used where the full-cycle period is used before. (Also observe, as noted before, that the load voltage amplitude is reduced by two diode drops.) For the 50\( \mu \text{F} \) case the P-P ripple estimate is \( \frac{\pi E}{\omega R_L C_L} \approx 1.4 \) volts. Compare this against the plotted data.

The upper of two plots following shows the contribution during each half-cycle to the overall load voltage. Except for the \( D_2 \) diode voltage drop \( v(2,3) \) is the load voltage during the positive half-cycle, while \( v(1,2) \) is the contribution during the negative half-cycle (except for the \( D_4 \) voltage drop). The overall load voltage is the sum of the two contributions. The lower plot displays the full-wave rectified load voltage concurrently with the sinusoidal source voltage.
Illustrative Problem: Bridge Rectifier

For this illustrative 'problem' the design objective is a simplified bridge rectifier, using the circuit discussed above. The AC voltage source provides a sinusoidal input of 12 volts amplitude @ 60 Hz. The load RL will vary in use so as to draw a current IL for which the bounds 4 ma ≤ IL ≤ 10ma are assured. The capacitor CF provides some filtering action, and additional filtering will be provided by the Zener diode (assuming of course that the design enables the Zener diode to operate appropriately in breakdown). The rectifying diodes to be used are 1N4004, and the Zener diode is the 1N5231. A preliminary design will be developed using idealized models for the diodes. It is no great inconvenience however to recognize a nominal 0.7 volt diode forward bias when conducting, and so the peak AC voltage provided by the rectifier will be approximately 12 - (2)(0.7) = 10.6 volts. The rectifier output voltage will vary as the capacitor is successively charged and discharged, as described elsewhere.

For the circuit to operate properly the Zener diode must operate in breakdown. Hence the rectifier must supply at least enough current to provide the minimum Zener 'keep alive' current and the maximum load current, and it must do this even when the voltage drop across RB is a minimum (low voltage of the ripple). Thus we must require \( V_{\text{low}} - V_Z \geq RB(I_{Z\text{min}} + IL_{\text{max}}) \), where \( V_{\text{low}} \) is the lower ripple voltage, \( V_Z \) is the nominal Zener voltage (Zener diode assumed to be in breakdown), \( I_{Z\text{min}} \) is the Zener 'keep-alive' current, and \( IL_{\text{max}} \) is the maximum load current. \( V_Z \) is 5.1 volts and \( I_Z \) is 20 ma for the specified diode, and we can choose \( I_{Z\text{min}} = 0.1*I_Z = 2 \) ma as a 'keep alive' requirement. Hence \( V_{\text{low}} \geq 5.1 + 0.012RB \). If we set \( V_{\text{low}} = 10.6 \) volts (as an upper limit) this would require \( RB \leq 458 \Omega \). Of course this implies an unrealistic assumption of zero ripple, but nevertheless it provides a meaningful upper limit value.

At another extreme the Zener diode must not carry excessive current at minimum load current; the worst case here occurs at the peak of the ripple when the voltage across RB is greatest. Hence \( V_{\text{high}} - V_Z \leq RB(I_{Z\text{max}} + IL_{\text{min}}) \) or \( 10.6 - 5.1 \leq RB(20 \text{ ma} + 4 \text{ ma}) \), and so \( RB \geq 229 \Omega \).

Just to get a feel for the numbers suppose \( RB = 250 \Omega \) (next highest ±5% standard value to 229) then we would find \( V_{\text{low}} \geq 8.1 \) volts. This would correspond to a peak-to-peak ripple of about 10.6 - 8.1 = 2.5 volts.

If we use \( RB = 250 \Omega \), which calls for a peak-to-peak ripple of 10.6 - 8.1 = 2.5 volts we can estimate the capacitor size needed from the approximate expression p-p ripple = \( V_{\text{high}} \) (period/RC). The period to use here is the half-cycle period (full-wave rectification), and so substituting find \( C \approx 141 \mu F \). A conservative capacitance of 250 \mu F is specified to assure the ripple is not too large. Note that a preliminary design always can be modified, and indeed a design generally should be reviewed with a view to possible technical, economic, and societal impact improvements. A PSpice analysis of the preliminary design provides a more precise computation of the expected circuit performance.

* Regulated Power Supply

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<th>3</th>
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<tr>
<td>DZ</td>
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<td>4</td>
<td>D1N5231</td>
</tr>
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* Declare a computational parameter called RVAL and give it a more or less arbitrary 
* default value of 220Ω. Then tell PSpice to obtain the value of this resistance to use in a 
* computation from a (later) description of RVAL to be provided as part of the listing.

```
.PARAM RLVAL = 220
RL 4 0 {RLVAL}
```

* The diode model descriptions following can be either saved in a file called (say) 
* FILES.lib and recalled into a netlist simply by including the statement .INC FILES.lib in 
* the netlist. This assumes the file is in the same folder/directory as the PSpice program; if 
* not use the *full address in the .INC * statement. These data are substituted into a 
* built–in diode equation in place of default parameters to closely approximate the behavior 
* of the diodes specified.

```
.MODEL D1N5231 D(Is=1.004f Rs=.5875 lkf=0 N=1 Xti=3 Eg=1.11 Cjo=160p + M=.5484 Vj=.75 Fc=. Isr=1.8n Nr=2 Bv=5.1 Ib=27.721m Nb=1.1779 + Ibv=1.1646m Nbvl=21.894 Tb=176.47u)
.MODEL D1N4004 D(Is=14.11n N=1.984 Rs=33.89m lkf=94.81 Xti=3 Eg=1.11 + Cjo=25.89p M=.44 Vj=.3245 Fc=. Bv=600 Ib=10u Tb=5.7u)
```

* Perform a transient analysis from 0 (implied) to 30 milliseconds and plot data at intervals * of 0.2 
* milliseconds.

```
.TRAN .2m 30m
```

* Step the value of the RVAL parameter declared above through the specific values listed. 
* PSpice will perform the transient analysis called for separately for each RVAL specified. 
* PROBE allows plotting the data for all runs either separately or in selected combinations. 
* You may wish to compute for a value of RVAL corresponding to a current larger than can 
* be supplied >if< the Zener operates in breakdown. In this case the Zener will operate 
* simply as a reverse-biased diode, and the load voltage will drop so as to enable a larger 
* current through RB.

```
.STEP PARAM RLVAL LIST 560 820 2.2K
.PROBE
.END
```

Data is computed for RL = 560Ω, 820Ω, and 1.2KΩ respectively; these draw load currents roughly from 
4ma to 10ma. Because the Zener diode operates in breakdown both the rectifier output voltage and the 
load voltage are insensitive (after an initial turn-on transient) to load current variations. The ripple at the 
load thus is reduced by the Zener action. Incidentally note that the ripple is roughly the expected value of 
about a volt or so.
In addition to the voltage plot the load, rectified, and Zener currents are plotted below for an 820 Ω load (load current of approximately 5.1/820 = 6.2 ma). The filtering action of the Zener diode is evident from the plot. Note: when plotting the Zener current take proper account of the implicit diode current polarity reference used by PSpice.

The first of the next two plots is a repetition of the 820Ω load resistance plot for the load voltage, except that the filter capacitor CF is reduced to 100 µF. As is to be expected the rectifier ripple roughly doubles, but the load voltage remains regulated. The Zener diode current changes, of course, to accommodate the increased range of rectifier output current. An advantage of the lower capacitance is reduced capacitor charging currents as well as a likely lower cost.

The second plot is for RL = 100Ω, for which case the Zener diode breakdown cannot be maintained. The diode operates in reverse bias drawing a negligible current, and the rectifier output voltage effectively is applied across a resistive voltage divider to provide a voltage of about 3 volts peak (10.6 *(100/350)) which tracks the ripple.
Circuits  Diode Rectifiers

Bridge Output Voltage
Load Voltage

$C_F = 100 \mu F$
$R_L = 820 \Omega$

Bridge Output Voltage
Load Voltage

$C_F = 100 \mu F$
$R_L = 100 \Omega$