**Complementary Symmetry Transfer Characteristic**

The purpose of this note is to compare the analysis of the circuit shown using the simplified PWL models, and a PSPICE nonlinear model computation. In particular the transfer characteristic will be evaluated.

The first formal step is to redraw the circuit diagram as illustrated below, i.e., create a new circuit whose behavior will be usefully approximate to that of the actual circuit.

**Cutoff**

There are four diodes, hence 16 conceivable combinations of diode states. Of these no more than five will occur. But more can be said. For example for \( V_{\text{in}} \) sufficiently negative Q1 will be cutoff, i.e., the emitter junction of Q1 will be reverse-biased. Moreover the collector junction also will be reverse-biased. The controlling condition for this is that \( V_{\text{in}} \leq 0.7\text{v} \). Similarly Q2 will be cutoff, since there is no path for base current flow. The PWL circuit is a bit misleading because the diode approximation is poor below the 'knee' of the diode characteristic. Refer to the actual circuit diagram to observe that the Q2 emitter junction voltage actually will be zero. Since there is no Q2 collector current \( V_{\text{out}} = 0 \) for \( V_{\text{in}} \leq 0.7\text{v} \).

**Linear Range**

When Q1 turns ON current also flows in Q2, i.e., both transistors operate in normal forward active mode. As shown beside the figure calculate \( I_{E1} \) from a KVL equation around the Q1 base-emitter loop. Anticipating \( \beta \gg 1 \) equate the Q1 collector current to the emitter current. Then calculate the Q1 collector voltage by neglecting the Q2 base current compared to the Q1 collector current. (These various approximations, however good they may be expected to be, should be verified against the results of applying the approximations.)

Use the calculated Q1 collector voltage to calculate the Q2 emitter current, and again anticipating \( \beta \gg 1 \) equate this to the Q2 collector current. The expression for \( V_{\text{out}} \) follows.
Saturation
Eventually, as the collector current of Q2 increases
Q2 will saturate. When this occurs the voltage
across Q2 will be (approx.) zero (see figure). This
occurs when

\[ V_{\text{out}} = \frac{12 - 0.7}{1.5 + 2.2} = \frac{2.2}{2.2} = 6.72 \, V \]

A PSPICE netlist to compute the transfer function follows.

```
CompPair Transfer Function
VS  1  0  DC  1
RS  1  2  10K
Q1  4  2  3  Q2N3904
RE1 3  0  2.2K
RC1 5  4  3.3K
Q2  7  4  6  Q2N3906
RE2 6  5  1.5K
RC2 7  0  2.2K
VCC 5  0  DC  12
.PROBE
.LIB EVAL.LIB
.DC VS 0 10 .05
.END
```
A PROBE plot of the transfer characteristic is drawn below. Superimposed are the estimates made for the three ranges of operation discussed. The following plot is for the transistor currents.

To illustrate the effects of saturation and cutoff a sinusoidal signal was applied, with amplitude as a parameter stepped through 1, 1.9, and 2.5 volts respectively.

The probe output voltage plot follows.