Introduction

Because transistor volt-ampere terminal characteristics are nonlinear details of the performance of a transistor in a circuit depends partly on the specific range of voltages and currents over which it operates. 'Biasing' of a transistor refers to the establishment of steady-state terminal voltages and currents which are the quiescent conditions from which subsequent changes are made. Appropriate steady-state voltage-current terminal bias conditions depend on the specific application involved, but at least one general characteristic can be inferred. Bias conditions should have an adequate degree of stability, so that the quiescent reference voltages and currents change little even if the circuit environment changes. There are three general methods, used separately or in combination, for approaching such stability.

Perhaps the most direct method conceptually is simply to prevent circumstances which would cause bias conditions to change, e.g., the environment in which a circuit operates can be controlled so as to constrain the causes of undesired changes. Controlling device temperature to stabilize temperature-sensitive parameters is an example of this method. This sort of control may take several forms. For example a circuit may be cooled with forced air circulation or refrigeration to improve heat removal; this may be combined with heat sinks to improve heat transfer from the device to a thermal reservoir and so more closely maintaining the device temperature at the temperature of the reservoir. Conversely a circuit may be heated in a temperature-regulated oven to maintain a fixed environment temperature. Similarly variations due to component manufacturing tolerances can be minimized by selecting matched components. However while it is an important topic with many ramifications environmental and selection control is not considered further for this experiment.

A second method is to establish a stable reference current or voltage (using, for example, environmental control or special devices and circuits dedicated to that purpose) and controlling the biasing relative to the reference. Such indirection can be more economically and technically advantageous than attempting to
control the environment of an entire circuit. The stable secondary reference is compared to the circuit voltage or current that is to be stabilized to detect changes in the latter, and appropriate circuit adjustments are made manually or automatically to reduce differences from the reference. This is common in integrated circuit designs, and an example will be examined in part in this experiment.

The third approach makes use of 'feedback', i.e., the circuit design utilizes inherently less sensitive circuit components connected in such a way that changes in a critical current or voltage automatically cause compensating changes. This is a very widely used technique, and is the principal one examined in this experiment.

**Approximate BJT 'DC' Circuit Model**

Easy to use computer programs for the analysis of electronic circuits with both linearized and nonlinear device models are widely available; sophisticated programs of this sort with considerable capability that not so long ago required 'mainframe' computers to operate now execute on inexpensive desktop computers with remarkable speed and accuracy. Generally however such programs are not overly useful in the initial stages even of relatively straightforward circuit designs. Quite often the circumstances of a design are such that there are more unknowns than there are circuit equations to solve, the circuit equations generally are nonlinear, often there are several design options to evaluate and selection from among the options involves judgement as well as computation, and almost always there are design trade-offs to consider. In such circumstances analytical precision is best partially sacrificed initially in favor of a comparatively imprecise but considerably simplified analysis which provides insight into the relationship between circuit performance and different circuit elements. It is important to recognize that 'imprecise' is not intended to suggest an arbitrary inaccuracy, but rather a degree of uncertainty which nevertheless provides a meaningful approximation. Determining the appropriate degree of approximation generally involves an application of judgement in a specific context; that comes with experience. Experienced or not trial and error calculations involving several design iterations frequently are involved. Once a trial design is formulated a more precise nonlinear computer analysis can be performed to fine-tune the design.

For this experiment (in particular) calculations of circuit bias performance will be based on the simplified transistor model illustrated in Fig. 7.1; the diodes have idealized characteristics. Note this model is not, nor is it intended to be, applicable for all possible transistor operating conditions. For example the model does not account appropriately for operation with the emitter junction reverse-biased and the collector junction forward-biased (inverted operation).

With the base-emitter junction forward-biased and the collector voltage $V_{CE} \geq V_{BE}$ the transistor operates in the 'normal forward active' region where transistor current amplification occurs.

The model approximates the actual device characteristics in this region by parallel lines. Saturation in the model occurs abruptly when $V_{CE} = V_{BE}$; the model is cutoff for a base-emitter voltage of less than $V_{BE}$. It is well worthwhile for you to compare the model characteristics shown with those of an actual device, qualitatively evaluating the nature of the approximations involved. The model can be made more accurate for specialized circumstances but, as these experiments will verify, the simplified model serves rather well for many general purpose operating conditions.

The elementary biasing arrangement illustrated in Fig. 7.3a serves for an example of the use of the model in making design judgements and estimates. The circuit diagram (center) replaces the canonical BJT icon
(which implies the non-linear terminal characteristics of the actual device) by the model assuming normal forward active operation, i.e., the (idealized) collector diode is open-circuit and the emitter (idealized) diode is short-circuit. Whether these assumptions are valid or not must be verified subsequently by noting whether calculated bias voltages and currents are consistent with normal forward active operation. From the model (and the idealized transistor characteristics it represents) equations (right) are obtained relating bias voltages and currents to the circuit parameters;

\[ I_C = \beta I_B = \frac{V_{BB} - V_{BE}}{R_B} \]

\[ V_{CE} = V_{CC} - I_C R_C \]

The equations suggest, for example, that variations in the emitter junction voltage will have a limited influence on the collector current if changes in \( V_{BE} \) are small compared to \( V_{BB} \). Emitter junction voltage variations due to temperature or manufacturing tolerances are relatively small, e.g., the junction voltage required for a given current decreases about 2 millivolt per °C increase in temperature. Hence if \( V_{BB} \) is much greater than one or two tenths of a volt the influence of the transistor emitter junction voltage in determining the collector current can be made quite small. Even if the exact value for \( V_{BE} \) is not known a modest uncertainty will not affect the calculation of the collector current significantly.

On the other hand the collector current is directly proportional to \( \beta \), a transistor parameter with a factor of 2 or 3 manufacturing tolerance, and a substantial temperature sensitivity. These variations will be reflected directly in the collector current, and because of this the circuit will not be particularly useful in biasing for normal forward active operation.

Note how semi-quantitative conclusions may be drawn from the idealized model which indicate the relative importance of different parameters in establishing quiescent operation, conclusions less readily apparent from the nonlinear characteristics.

**Biasing from a Reference**

The biasing arrangement illustrated in Fig 7.4, is a simplified version of an arrangement used in more sophisticated form in many integrated circuits. A relatively stable reference current flowing through T1 is established, and this reference is used to maintain a similarly stable T2 transistor current. T1 is operated with zero collector-base voltage, i.e., as a 'diode-connected' transistor. Operating with zero collector-base voltage insures the transistor will not saturate since the collector-base junction can't become forward-biased.

As will be seen the collector currents of the two transistors will be nearly equal, and assuming a reasonably high \( \beta \) the base current drain by T2 on the collector current of T1 is small, i.e., T2 has little influence on the collector current of T1. If the transistors T1 and T2 are physically identical, their respective emitter currents will be substantially the same since the emitter junctions share a common voltage difference. With \( V_{CC} \) large compared to the T1 emitter junction voltage (about 0.7 volt for a silicon device) the T1 collector current is determined primarily by \( R_C1 \) and \( V_{CC} \). Thus the stability of the T2 biasing is not greatly
dependent on \( T_2 \), but rather depends on the more easily controllable supply voltage \( V_{CC} \) and the intrinsically more stable resistance \( R_{C1} \).

**Experiment 7.1**

Assemble the circuit described above using \( R_{C1} = R_{C2} = 2.2 \, k\Omega \). However in place of a common voltage supply use separate variable voltage supplies. Set the voltage for the \( R_{C2} \) branch at 15 VDC; adjust the voltage for the \( R_{C1} \) branch to make the collector voltage of \( T_2 = 7.5 \) volts. Compare the experimental \( R_{C1} \) branch voltage setting to the estimated value you calculate using the simplified circuit model for a BJT described before.

Carefully heat the circuit (using a hair dryer supplied by the lab instructor), and observe the effect on the collector voltage of \( T_2 \). Is the bias current stable?

Allow the circuit to cool to room temperature. Then disconnect \( T_1 \) (but not \( R_{C1} \)) and note the effect on the collector voltage of \( T_2 \). In your report describe and explain your observations. Is the assumption of operation in normal forward-active mode appropriate? Heat this circuit as before and note the effect on the collector current.

With \( T_1 \) still disconnected increase the \( T_2 \) base resistance \( R_{C1} \) from 2.2 k\( \Omega \) to 220 k\( \Omega \). Observe the collector voltage as the circuit is heated again. Describe and explain your observations, comparing them to those of the previous measurement.

**Emitter-Stabilized Biasing**

The emitter-stabilized circuit configuration illustrated in Fig. 7.5 (with 'single-battery' biasing) uses an emitter resistor to reduce the dependence of the emitter (and so collector) current on the transistor parameters. Stabilization is obtained by a circuit reaction to changes in emitter current in such a way as to mitigate those changes. This circuit arrangement is analyzed in detail elsewhere.

The \( R_1 - R_2 \) biasing network is used to hold the base-ground voltage at an approximately constant value. This is accomplished by designing the base current to be a small part of the total current through \( R_1 \), since then variations in transistor base current will have a small influence on the voltage drop across \( R_1 \). If the emitter were connected directly to ground however such base-current variations would affect the emitter current quite a bit; the base current variation is amplified by a factor of \( \beta + 1 \). With the emitter resistor added emitter current changes produce corresponding changes in the voltage drop across \( R_E \). For example an increase in emitter current increases that voltage drop. But an increase in this voltage drop causes a reduction of the base-emitter voltage, since the base voltage is held substantially constant. The consequence of this is to reduce the emitter current, i.e., the reaction to an increase of emitter current is to cause a junction voltage change which acts to reduce the increase. A net emitter current increase will remain, of course; a reaction implies at least some residue of the original action to react to. However the net increase will be less, substantially less with proper design, than would occur otherwise.

**Experiment 7.2**

Before coming to the laboratory design a single stage emitter-stabilized biasing circuit to operate with a nominal collector current of 1 milliampere, and a nominal collector voltage of 9 volts, with \( V_{CC} = 15 \) VDC. Assemble your design and determine the bias voltages and currents. Are your measured values the expected ones? In your report describe your design and account for any differences between calculated and measured values.
Use the hair dryer as a hot air source to heat the transistor, monitoring either the collector or emitter voltage as you do so. Allow an equilibrium to be reached. Comment meaningfully on the bias stability observed. For example estimate the changes that you would expect if $\beta$ were half its 'typical' value, and if it were twice the typical value. Did the observed changes remain within these limits?

Replace the collector resistor you are using for your design with one which has (approximately) three times the resistance. Measure the collector voltage and in your report explain the measurement. Why did the emitter stabilization fail? Is the analysis on which your design calculations are based valid? If not why not?

In addition to the comparisons and explanations called for the report shall include a brief description of the sequence of steps used in developing the design. Each 'step' shall consist of a short statement of the purpose/objective of the step, any calculations involved, and for every instance where a design choice of a parameter value is made a meaningful reason for the particular choice made. As an (arbitrarily composed) rough illustration:

Step # xx: Select a trial value for $R_E$. Make the emitter voltage large compared with expected variations in the base-emitter voltage to limit the effect of these changes on the emitter current. Estimate junction voltage changes for a silicon device at a total of 0.2 volts over 100°C temperature change. Choose the emitter voltage large compared to this variation, but not so large as to limit the possible collector voltage swing; say $\approx 20 \times 0.2 = 4$ volts. For a 1 milliampere current this makes $R_E \approx 4$ kΩ. A standard 5% value of 3.9 kΩ is used for first design pass.

**Collector-Stabilized Biasing**

Emitter stabilization references changes in emitter voltage to a (nearly) fixed base voltage. A closely related although generally less advantageous stabilization method is to reference changes in the base voltage to a fixed emitter voltage, as in the circuit drawn in Fig. 7.6. The emitter reference voltage in this circuit happens to be the ground voltage.

If there is a change, say an increase, in current through $R_C$ (this current is equal to the emitter current) the collector voltage decreases. Hence the base current will decrease, and this will decrease the emitter current. The reaction is such as to mitigate the original current change.

Application of KVL (and superposition) using the simplified BJT DC model relates the change in emitter current to the corrective change produced in the junction voltage;

$$\Delta I_E \left( R_C + \frac{R_B}{\beta+1} \right) = \Delta V_{BE}$$

Note the appearance of the $\beta+1$ factor, reflecting the relative values of the base and emitter currents. To reduce the influence of $\beta$ the resistance of $R_C$ should be suitably large compared to that of $R_B$.

Unfortunately this means the voltage drop across $R_C$ should be relatively large, with the indirect consequence of limiting the range over which the collector voltage can be varied by a signal to be amplified. Collector stabilization is not used often directly. However it is used in conjunction with emitter stabilization in a multi-stage biasing configuration of a sort illustrated later.

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**Biasing Pairs**
A number of biasing circuit configurations of interest involve the use of two transistors.

a) Capacitor Coupling

The circuit diagram drawn in Fig. 7.7 is that of a classical capacitor-coupled two-stage common-emitter amplifier. The capacitor is used to decouple, i.e., isolate, the DC collector voltage and current of the first stage from the DC base biasing for the second stage. With the DC interaction between stages removed a design which otherwise would have to reconcile operating requirements for both stages concurrently can consider them individually. There is a price for this simplification however. The reactance of the coupling capacitor will increase as the signal frequency fed into this amplifier decreases. This reactance is in series with the second stage input impedance, degrading the signal transfer from the first stage into the second. The higher the coupling reactance the greater the fraction of the signal voltage at the collector of the first stage dropped across the capacitor. Thus the coupling introduces a signal transfer attenuation which becomes increasingly severe as the frequency is lowered. Even with large values of coupling capacitance, and there are practical constraints limiting capacitor size, there is a frequency below which circuit performance is degraded unacceptably. This represents a limit on the range of operation of the amplifier. For integrated circuits capacitor coupling problems are aggravated by the relatively large (and consequently expensive) surface area required for monolithic capacitors. DC coupling, i.e., coupling stages without the use of frequency-sensitive components such as a capacitor, is commonly used in integrated circuits. Then, of course, the biasing of one stage is no longer independent of another and this must be taken into account.

Unfortunately the added difficulties of interstage interactions that come with simple direct coupling of cascaded amplifier stages quickly become intolerable. For example since the base voltage must be lower than the collector voltage for unsaturated operation simple cascading of successive DC coupled stages requires successively higher collector voltages. This limits the range of variation of collector voltage for the last stage, which is where it would likely need to be greatest.

b) Complementary Pair

One technique for overcoming this voltage escalation makes use of alternate NPN and PNP transistor stages, as illustrated in Fig. 7.8. In this example the first stage, using an NPN device, is biased using emitter stabilization. In fact the second PNP stage also uses emitter stabilization. But the polarity of the terminal voltages for proper biasing means the PNP emitter should have a higher voltage than the NPN collector voltage. Moreover a third NPN stage would have its base connected to the PNP collector, which is at a lower voltage. Thus complementary transistor voltage 'level shifting' up and down by alternate stages avoids the problem of monotonic shifting, at the 'cost' of using two transistor types.

An approximation useful in estimating circuit bias parameters is to assume the T2 base current is negligible compared to the T1 collector current. This usually will be a good approximation because the the two stages generally will have collector currents roughly of the same order of magnitude. The approximation enables the biasing calculations for T1 to be made independent of T2. Then the T1 collector voltage provides the base bias voltage of T2. The difference between this voltage (and the junction drop) and VCC determines the current through RE2, which is the T2 emitter current. Note that the output is taken from the collector of T2.
If only as a matter of good practice, and it is really more than that, approximations such as that for the base current no matter how likely their validity should be verified against numerical results of the analysis in which they are used. In other words check to see if the numbers calculated are consistent with the approximations used to calculate them. Is the calculated base current to T2 in fact actually small compared to the calculated collector current of T1? Once consistent 'ballpark' values are determined a computer analysis can be performed for greater accuracy.

For increased accuracy of the approximate calculation, not often really necessary but worth noting, the calculation can be iterated, i.e., use the calculated T2 collector current to provide an estimate of the T2 base current and repeat the calculation using this current estimate instead of simply neglecting the base current. It can be shown that the circuit behavior is such that such an iterative calculation converges (ordinarily very rapidly) to consistent results.

c) Shunt-Series Pair
The circuit in Fig. 7.9 is an interesting (and useful) combination of both emitter and collector stabilization, one of several such associations alluded to previously. Suppose, for the purpose of discussion, that RB is connected from the base of T1 to the collector of T1 rather than to the emitter of T2; this then would be the collector stabilization configuration described briefly earlier. The collector of T1 is connected to the base of T2, and since the T2 base voltage will not change much even for large current changes (forward-biased junction), changes in the T2 emitter voltage should be very nearly equal to changes in the T1 collector voltage. Hence connecting RB to the T2 emitter should have very much the same circuit effect as connecting it to the T1 collector. In other words in effect T1 will be collector-stabilized indirectly. As it happens the illustration shows T1 with emitter stabilization also, assuming RE1 is not zero.

If T1 is stabilized then the base bias of T2 is held nearly constant, since it provided from the collector of T1, and RE2 then provides T2 with emitter stabilization. This combination of DC coupled stages often is called a 'shunt-series feedback pair'. The label, whose more subtle connotations will become clearer at a later time, is a formal description for 'collector-emitter stabilized pair'.

Approximate analysis of this transistor pair is simplified considerably by neglecting (as always subject to subsequent verification of the consistency of the calculations) the T2 base current and writing a voltage equation in terms of the T1 collector current through RC1, the emitter junction voltage of T2, RB (express the base current in terms of the T1 collector current), the emitter junction voltage of T1, and finally RE1 (express the emitter current in terms of the T1 collector current). This provides an equation with one unknown, the T1 collector current. Note that it is the β of T1 only that is involved in this equation.

Once the T1 collector current is calculated the T2 base voltage can be calculated, and from this the T2 emitter current. All other voltages and currents then follow. As before iteration, using the calculated emitter current of T2 to provide an estimate of the T2 base current, can be used to converge rapidly to consistent results. Usually this is not at all necessary, and rarely would more than one iteration make any significant difference. But it could.
d) Series-Shunt Pair

The DC-coupled bias configuration illustrated in Fig. 7.10 is less easily interpreted than the preceding case. The first stage is emitter stabilized by $R_{E1}$ (the DC base voltage source connected through $R_B$ is not shown explicitly. $T_2$ also is shown emitter-stabilized, although $R_{E2}$ can be zero. It is an indirect collector-base stabilization of $T_2$ by $R_F$ that provides the 'shunt' part of the characterization of this biasing pair.

To recognize the 'shunt' character of the connection note that $R_{E1}$ actually acts to stabilize not the $T_1$ emitter current but rather the sum of that current and the current through $R_F$. It is the total current through $R_{E1}$ that produces the voltage at the emitter of $T_1$. However the emitter voltage of $T_1$ remains substantively constant, varying just slightly to provide the small junction voltage changes that adjust for changes in current through $R_{E1}$. Hence the current through $R_F$ reflects changes in the collector voltage of $T_2$. These changes cause equal (roughly) changes in the $T_1$ emitter/collector current to keep the current through $R_{E1}$ constant (roughly). Hence the base voltage of $T_2$ changes, and the polarity of the change acts to offset the causative $T_2$ current change. The effect is essentially that obtained by connecting $R_F$ to the base of $T_2$ directly, except for the DC voltage offset provided by connecting to $R_{E1}$.

This circuit ordinarily would be designed so that the current through $R_F$ is small compared to the current through $R_{E1}$; in effect this allows the stabilization of $T_1$ to be done more or less independently of $T_2$. The stabilization of $T_2$ then is consequent to $T_1$ being stabilized. To analyze this circuit assume this has been done for an initial calculation, i.e., neglect the $T_2$ base current and the current through $R_F$ to calculate $T_1$ voltages and currents. Then calculate $T_2$ voltages and currents. The adequacy of the assumptions made should be verified, and if necessary improve the analysis by a recursive calculation, i.e., use the (approximate) current through $R_F$ calculated as an estimate instead of neglecting this current. Convergence is rapid for a design providing even marginal stability.

e) Darlington Pair

Two transistors connected as a cascade of CC stages, as shown in Fig. 7.11, form what is often called a a 'Darlington' pair'. Strictly speaking the Darlington name applies to the special case in which $R_{E1}$ is removed, so that the emitter current of $T_1$ in its entirety supplies the base current of $T_1$. However $R_{E1}$ is used to 'bleed' some of the $T_1$ emitter current away from the $T_2$ base, enabling $T_1$ to operate at a modest current level without saturating $T_2$. Even with bleeding this easily designed bias configuration provides a higher current gain than a single stage.

$T_2$ is emitter-stabilized much the same as a single transistor; the overall emitter junction voltage here is roughly twice that for the single device circuit. Neglect the $T_2$ base current for the bias calculation. $T_1$ is stabilized indirectly, i.e., the voltage across $R_{E1}$ is one diode drop higher than the emitter voltage of $T_2$. This circuit provides a high input resistance. In this respect it is interesting to note that the incremental collector-emitter resistance of $T_1$, which is of the order of megohms and almost always negligible elsewhere, here provides the ultimate limitation on input resistance since it shunts $R_{E1}$. 
f) **Differential Amplifier**

The differential amplifier configuration shown in Fig. 7.12 uses symmetry to discriminate between 'common-mode' and 'differential-mode' signals. Equal (common-mode) signals applied to the base inputs produce equal output signals, and the difference signal is (ideally) zero. The discrimination actually is even stronger because the transistor in the emitter path acts as a current source, i.e., a very high resistance, to provide effective stabilization against common-mode current changes. However if the base signals are out of phase (differential-mode) so are the amplified collector signals, and the difference signal has twice the amplitude of either collector signal alone. Moreover differential-mode emitter current changes do not flow through T3, and there is no gain-inhibiting stabilization of the changes.

DC biasing of the differential pair is straightforward; T3 is emitter-stabilized and the presumed symmetry of T1 and T2 causes the collector current of T3 to divide equally between T1 and T2.

g) **CE-CB Pair**

The 'cascode' BJT pair illustrated in Fig. 7.13 offers certain advantages for high frequency amplification; it consists of a CE input stage followed by a CB stage. The CE stage is used for current amplification, while the CB stage is an impedance transformer with reduced interaction between the emitter and collector voltages. The circuit uses capacitors to reconfigure the incremental circuit from the DC biasing arrangement. Thus the '$\infty$' capacitor designation refers to a capacitance value large enough at the lowest frequency of interest so that the capacitor reactance is small enough to be considered a virtual short-circuit for incremental signal changes. Note the implication of a low-frequency cutoff for the amplifier response. Note also that T1 is emitter stabilized, and the emitter current of T2 necessarily equals the collector current of T1. This circuit is pedagogically useful for testing your understanding of incremental circuits.

**Design Experiment 7.3**

This is a paper experiment. Design a shunt-series amplifier pair with a nominal collector current of 1 ma for each transistor. VCC is to be 10 volts, and the collector voltage of the second stage is nominally 7.5 volts. In your report document your design carefully and fully, including a computer analysis to determine the bias voltages and currents.