Objective
The objective of this experiment is to examine the distinctive low-frequency incremental-parameter transfer properties of the three basic single-stage transistor configurations; Common Emitter, Common Base, and Common Collector. Experimental measurements of the salient characteristics of each configuration are compared with theoretical expectations, and their performance is evaluated in terms of general circuit principles.

Parts List
BJT 2N3904
resistors 56Ω, 560Ω, 1kΩ, 5.6 kΩ, 10kΩ, 82 kΩ
capacitors 0.2 µfd, 5 µfd

Two-Port Insertion Gain
The three circuits considered in this experiment, described in further detail below, should be reviewed before the beginning of the laboratory period assigned for this experiment to refresh information needed for the proper conduct of the experiment. Failure to do so almost certainly seriously compromises the likelihood of satisfactorily completing the experiment, and certainly makes it much more difficult. Read the experiment for details.

The generic circuit configuration used for this experiment is drawn as Fig 10.1. The voltage source and resistor on the left represent the Thevenin equivalent of an input source circuit. The resistor to the right is the 'load' across which the output voltage $V_o$ is measured. Between the two a two-port network is connected to modify the voltage transfer from the source to the load from what it would be with a direct connection.

The simplest situation is that for which the two-port transfer network is comprised simply of two wires, providing a 'straight-through' connection from the source to the load. The voltage transfer 'gain' in this case is

$$\frac{V_o}{V_i} = \frac{R_o}{R_i + R_o}$$

If $R_o << R_i$ the voltage transferred is a small fraction of the source voltage, i.e., the voltage 'gain' is considerably less than one. For this experiment the resistors are deliberately chosen to make the voltage gain for the direct connection much less than one. The 'straight-through' two-port circuit provides a convenient reference against which to evaluate the effect of inserting other two-ports on the voltage transfer.
fraction, specifically single-stage bipolar junction transistor amplifiers. The diagram below uses a simplified equivalent circuit for a voltage amplifier to illustrate the general nature of the modified conditions.

The input resistance of the amplifier equivalent circuit is $R_1$; the reverse-transfer from output to input is neglected (and is negligible for this experiment). The amplifier provides a voltage gain $A$, and has an output resistance $R_2$. A straightforward calculation obtains

$$\frac{V_0}{V_1} = \frac{R_1}{R_1 + R_1} \times \frac{A}{R_1 + R_1}$$

As the partitioning of the equation suggests the two-port influences three aspects of the voltage transfer from source to load. The first term describes the input transfer, i.e., how efficiently the source transfers voltage 'into' the two-port. The second term corresponds to the voltage transfer internal to the two-port itself, and the third term expresses the efficiency of the output transfer from the two-port to the load. Depending on the specific two-port circuit any or all of these factors may provide a significant improvement (or degradation) for the overall voltage transfer, as compared to the 'straight-through' transfer gain.

**Experiment 10.1**

In this experiment the three basic single-stage transistor amplifier configurations are used, each in turn, as the two-port network inserted between the source and the load. Each circuit is to be analysed beforehand to determine a theoretical incremental voltage transfer expression. This theoretical expression should be compared to the 'straight-through' reference gain, with specific attention to the influence of the transistor circuit on the three factors described for the reference direct connection case.

Each circuit considered is to be assembled and measured voltage gains are to be compared with theoretical calculations for an evaluation of expectations vs achievements. After all three configurations have been examined an overall evaluation of the three circuit configurations shall be made, with particular note made of the special advantages offered by each.

**CE amplifier**

The Common Emitter amplifier circuit to be used in the experiment is drawn as Figure 10.3. Calculate the DC quiescent point voltages and currents expected using nominal device parameters and the simplified PWL model. A prior computer computation also shall be made. Compare computed bias values to measured values in the laboratory; if there is a serious discrepancy further measurements are of little if any value. Check the circuit connections.
The base coupling capacitor is indicated as having \( \infty \) value, meaning that its value is to be large enough so that at a frequency of a few kilohertz the capacitive reactance is small compared to 1 k\( \Omega \). The capacitor then provides a DC blocking action isolating the source from the biasing circuitry, but has a negligible influence on the source impedance for higher frequencies. Similarly the emitter bypass capacitor reactance at the same frequency should be small compared to 560 \( \Omega \). The emitter resistance therefore provides DC feedback stabilization but is effectively bypassed at higher frequencies. The exact capacitance values are otherwise not critical. Note that two measurements are indicated for this circuit in the figure, one with an \( \infty \) (large) emitter 'bypass' capacitance and the other with that capacitor removed.

The experimental signal source is formed by the laboratory signal generator shunted by a 56 \( \Omega \) resistor as illustrated by Figure 10.4. The shunt assures an overall laboratory source output resistance which is low compared to the 1 k\( \Omega \) resistor placed in series to complete the Thevenin equivalent circuit for the source.

Use a nominal signal frequency of 10 kHz for your transfer gain measurements; use the oscilloscope to make a rough check to assure 'midband' frequency operation, i.e., operation at a frequency for which modest changes in frequency do not change the transfer gain. The simplified incremental-parameter equivalent circuit drawn to the right is adequate for the calculations and interpretations to be made.

Compare the calculated voltage gain to the measured gain (and the computed gain) for the two cases \( C = \infty \), and \( C = 0 \). Include details of the gain calculations and the comparisons in your report.

**CB Amplifier**

This experiment essentially parallels the preceding one, except that the amplifier circuit is the Common Base configuration of Figure 10.6. Note that the DC biasing circuitry is exactly the same as for the CE stage; you can use that circuit assembly as a starting point for this one instead of disassembling the one before assembling the other. One modification is the base-to-ground capacitor used to electrically 'short-circuit' the base to ground in the incremental equivalent circuit; estimate an adequately large practical value to use for the \( \infty \) capacitance specification; state the basis of your estimate along with the capacitor value used in your report.
Another modification from the preceding CE configuration is to connect the incremental input signal source between the emitter and the base. The incremental output is taken between the collector and the base. Your report should make clear the distinction between the physical connections and the incremental equivalent circuit electrical connections for the input and the output. Be sure to include an incremental circuit diagram in the report, along with details of the voltage gain calculation.
**CC Amplifier**

Perform the same basic experiment again but use the Common Collector configuration; a circuit diagram is drawn as Figure 10.7. Note that the 5.6 kΩ collector resistor present in the previous two experimental circuits is replaced by a short-circuit here. Note also that the incremental output is taken between the emitter and the (grounded) collector, while the incremental input is between the base and the (grounded) collector.

Your report should make clear that you understand the distinction between the physical connections and the incremental equivalent circuit electrical connections for the input and the output. Be sure to include an incremental circuit diagram, along with details of the voltage gain calculation.

**General Remarks**

The simplified incremental parameter transistor model to be used in circuit calculations for this experiment is redrawn to the right, configured so the input on the left is between the base and emitter and the output on the right is between the collector and the emitter, i.e., a CE configuration. It follows directly from the circuit diagram that the input resistance is $r_{be}$ (typically a few kilohms or so), and perhaps less directly that the load resistance should be low preferably compared to the collector resistance of the test circuit to transfer current into the load efficiently. This configuration offers the possibility of either current or voltage gain.

The self-same circuit is redrawn to the left in a CB configuration, input on the left and output on the right. The input resistance of this configuration is lower than for the CE configuration because of the transistor action. The input current is $(\beta+1)i$, while the input voltage drop is $ir_{be}$, i.e., produced by a smaller current. Hence the input resistance is $r_{be}/(\beta+1)$, rather than $r_{be}$ as in the CE configuration.

The transistor action as represented by the current source siphons most of the input current away from $r_{be}$. The current gain is $\beta/(\beta+1)$, approximately 1 for typical values of $\beta$. Hence current gain is not realizable, but voltage gain is available. Incidentally both current reference arrows have been reversed from what they would be by simply 'bending' circuit branches to reconfigure the model. This is of course a cosmetic change which has no electrical consequence.

The properties of the CC configuration drawn to the right (Fig. 10.10) are more easily inferred if a load resistor is imagined to be connected between the collector and the emitter (which is on the right). The resistance of the load resistor appears magnified to the input source. The source supplies a current $i$, but the transistor action increases that to $(\beta+1)i$ for the load current. Hence the voltage drop across the load resistor is greater by a factor of $\beta+1$ than what would be produced by the source current alone, and because of this the source 'thinks' the load resistance is larger than it is by the same factor. The CC configuration provides a current gain as noted. However the voltage gain always is less than 1, since the input voltage is greater than the output voltage by the drop across $r_{be}$. 

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Figure 10.7 CC amplifier

Figure 10.8 BJT model; CE configuration

Figure 10.9 BJT model; CB configuration

Figure 10.10 BJT model; CC configuration