Objective
This is an introductory experiment to examine several aspects of bipolar transistor switching with capacitive and inductive loads.

Capacitive switching
Capacitance is an electrical parameter measuring the ability of a device to store and maintain separated positive and negative electrical charge. The work necessary to separate the charges is reflected in the strong Coulomb attractive forces between the separated charges, and in the work that these forces can do if a path is provided which enables the charges to recombine. Charge storage effects are intrinsic in semiconductor junction devices. A transistor equivalent circuit, for example, includes nonlinear junction and diffusion capacitance components corresponding to internal charge separation and redistribution effects. The time needed to modify internal charges associated with these capacitances so as to change the electrical state of a transistor affects the ability of the transistor to respond to fast input signal changes. If the terminal voltages change too fast the transistor is not able to respond internally fast enough for proper circuit action to occur.

For this experiment however signal rates will be much slower than the intrinsic response speed of the transistor, i.e., internal charge distributions effectively occur instantaneously compared to the time needed for significant terminal signal changes. The controlling capacitive factors for this experiment are circuit components external to the transistor. External capacitances inevitably are present as parasitic circuit elements, and capacitance often is added specifically to produce certain effects. For this experiment capacitors are intentionally added to the circuit to dominate parasitic capacitances and make it easier to relate theory and experiment.

Capacitive circuit components ordinarily are linear or nearly so, i.e., the charge stored by a capacitor (equal, oppositely signed charges) is directly proportional to the voltage across the capacitor (work per unit charge done by recombining charge); the proportionality constant is the capacitance. This is the basic linear capacitor studied in introductory circuit theory courses. A principal objective of the first part of this experiment is to provide direct experience with and better understanding of capacitive effects when a transistor is used as a switch, i.e., the transistor either is turned 'ON' (almost always saturated) or turned 'OFF' (cutoff).

There are principally two considerations to keep in mind about capacitors. First: a charged capacitor stores energy and, since energy does not vanish spontaneously, the stored energy must be removed somehow in order to discharge the capacitor. Since the voltage across a capacitor is proportional to the capacitor charge it follows that to change the voltage the stored charge must be changed. Increasing the charge increases the
voltage, and vice versa. Changing the stored charge involves a charge transport, i.e., either removing charge from or adding charge to the capacitor. Charge transport is what an electrical current provides. The relevant equations are

\[ q = C \cdot v, \]

and its differential form

\[ i = C \cdot \frac{dv}{dt} \]

where \( q \) is the charge magnitude, \( i \) is the rate of change of the charge, i.e., the current, \( v \) is the voltage difference across the capacitor, and \( t \) is time. The proportionality constant \( C \) is the capacitance.

The second important consideration follows from the presumption that infinite currents do not occur in practice. Therefore in the course of changing a stored charge with a finite current a finite interval of time must pass. Equivalently, a finite interval of time is necessary to change the voltage across the capacitor. How long a time is needed depends on the details of the circuit in which the capacitor is imbedded. Recall, for example, that in a circuit containing a single capacitor and a resistor the voltage across the capacitor changes exponentially, and that the circuit time constant is the product of the capacitance and the Thevenin (or Norton) equivalent resistance 'seen' by the capacitor.

The circuit diagram drawn to the right (Fig. 20-1) is used in this experiment to illustrate various aspects of capacitive switching behavior. Initially the 'loading' capacitor tied to the transistor collector is to be deactivated, i.e., assume the switch is open (or just don't connect the capacitor at all).

In a steady-state condition, with no signal applied through the 0.1\( \mu \)f base coupling capacitor, the transistor is biased ON, and it is a straightforward matter to verify that the transistor will be saturated for the experimental circuit parameter values shown. (For example observe that the ratio of base resistance to collector resistance is less than the nominal transistor \( \beta \approx 120 \), consider the relative currents in the two resistors, and follow this thought through to the conclusion noted.)

A positive-going square wave signal of amplitude \( \Delta V_b \) is applied to the base input. The pulse width is to be selected experimentally so that all transients generated by the change of voltage at one pulse edge have 'settled' into a steady-state condition before the other pulse edge occurs; the circuit therefore effectively is in a steady-state condition when either pulse edge occurs. A repetitive signal so organized enables convenient use of an oscilloscope to view concurrently but effectively independent of one another transient phenomena generated on the rising and falling edges of the input pulse train respectively.

On the rising edge of an input pulse the voltage at the input side of the base coupling capacitor is 'pulled up' rapidly by \( \Delta V_b \) volts. The voltage across the capacitor changes essentially immediately, i.e., the capacitor charges with a very small time constant. The Thevenin resistance 'seen' by the input capacitor is the parallel combination of \( R_B \) and the equivalent resistance of the forward-biased base-emitter junction. The latter, while not a constant, is of the order of a few ohms. (Alternatively note that, because the transistor is saturated and so operates with a more or less fixed collector current, a rise in base voltage of 50 millivolts or so increases the charging current by an order of magnitude.) Hence for the 0.1\( \mu \)f capacitance the charging time constant involved is of the order of a few microseconds. This is a very short time compared with other characteristic circuit times involved in the experiment, and because of this a new steady-state condition establishes itself essentially immediately. Note also that the voltage change is all on the signal source side of the capacitor. A very small voltage 'pip' in the base voltage waveform may be observed on some oscilloscope displays corresponding to the slight temporary increase in emitter junction voltage to accommodate the capacitor charging current. The net effect of the rising-edge transient therefore is simply to charge the capacitor without significantly affecting the saturated transistor otherwise.

Incidentally there is an implicit assumption that \( \Delta V_b \) is greater than the forward-bias voltage of the base-emitter junction; this is significant later.
The situation is quite different for the negative-going edge of the input pulse. The input voltage of the base capacitor is 'pulled down' by $\Delta V_b$ volts immediately, as illustrated in the graph below. However if the voltage across the capacitor is to change current must flow through the 22 k$\Omega$ base resistor; the direction of the current flow required does not permit a significant current flow through the base-emitter junction. The time constant involved now is considerably larger than before, and the voltage across the capacitance can't change anywhere near as fast as the pulse fall time. Hence as the input pulse voltage drops so also does the voltage on the base side of the coupling capacitance. This drop in voltage reverse-biases the base-emitter junction (assuming $\Delta V_b$ is large enough), and as a consequence the transistor is cut-off immediately.

The capacitor immediately begins charging through the base resistor. A formal analysis will provide the same result as is obtained here by reasoning from general information. The charging is in a single time-constant RC circuit, and so the base voltage changes exponentially; the solution of a linear first-order differential equation with a constant driving force (i.e., RC charging by a DC source) has the form

$$\text{base voltage} = A + Be^{-t/RC}$$

The final base voltage reached as $t \to \infty$, assuming the cutoff condition of the transistor does not change, is the collector voltage of 10 volts. The initial voltage is the junction forward-bias voltage less the pulse height; call this difference $-V_0$ as shown in the figure to the right. Then

$$\text{base voltage} = 10 - (V_0 + 10) e^{-t/RC}$$

This is the exponential rise sketched in Fig. 20-2.

The sketch also indicates that the exponential increase stops well short of 10 volts. This is because the calculation assumes the transistor is cut-off. However the electrical configuration of the charging circuit changes when the base voltage becomes large enough to turn the transistor on again. With the junction forward-biased the base voltage is 'locked' at a nominal 0.7 volts, and there is no further charging. Set the base voltage to 0.7 volt in the exponential expression and solve for the time interval $t$ between the transistor cutoff and the resumption of conduction; this period is to be verified experimentally.

**Experiment # 20.1**

Connect the circuit as shown in Gig. 20-1, excluding for the moment the output loading capacitor. (Remember to offset the input pulse train to have zero baseline voltage.) Obtain an oscilloscope display of the base voltage on one channel, and concurrently arrange to display either the input pulse train or the transistor collector voltage on the other channel. This will enable measurements using a common time scale for all waveforms. Make appropriate measurements of the input pulse amplitude and width, the base voltage, and the collector voltage pulse width and amplitude. Note that there are three critical (relative) times: the time of the falling edge of the input pulse when the transistor is first cutoff, the time at which the transistor turns on again, and the time at which the following rising edge of the input pulse occurs. In order to avoid interference between successive input pulses the base transient must be completed before the next transistor cutoff occurs. (You may wish to try, as an optional part of the experiment, decreasing the period of the input square wave and observe the effect of retriggering the base cutoff prematurely.) Compare the base waveform amplitude and time measurements to calculated values; include a sketch on the same time scale of one period of the base and collector voltages. Describe and explain the relationships between these voltages. Include a computer transient analysis as part of your report.

After completing the first part of the experiment, connect the collector loading capacitor; use the same capacitor size as used on the input, i.e., 0.1 $\mu$F. When the transistor is cutoff on the falling edge of the base pulse the collector voltage initially is low, since the transistor was saturated. With the transistor cutoff the
collector loading capacitor begins charging through the collector resistor. Observe the change in the collector voltage rise time from what it was before the capacitor is added; calculate the rise time and compare to the observed value. What happens to the collector waveform if the collector charging time constant is comparable to the base switching period? Change the loading capacitor to about 1 µf and compare the observed effect with your prediction of what it would be.

The fall time considerations for the collector voltage are a little more involved because when the transistor is turned on it provides a relatively high current discharge path for the capacitor. Assume that the collector capacitor becomes fully charged during the time the transistor is cutoff. When the transistor is turned on again (eventually) the loading capacitor prevents the transistor from being immediately saturated even though a large collector current flows. If that current flowed through the collector resistor then indeed the collector voltage would drop and the transistor would saturate. However the capacitor must be discharged first in order to lower the collector voltage. Hence initially and momentarily there is no current at all through the collector resistor! There is a very large collector current but the current is supplied initially entirely from the stored capacitor charge. As the capacitor discharges the collector voltage drops and current flow through the resistor increases, i.e., the capacitor provides less and less of the collector current and current through the resistor provides more and more. Eventually a steady-state is reached in which the transistor is saturated and the capacitor is essentially fully discharged. This steady-state ordinarily is reached very quickly because the collector current is quite large; recall that the base current is relatively high. Incidentally note that it is not the high base current per se that causes saturation. Rather it is the lowering of the collector voltage because of the voltage drop across the collector resistor. The high base current assures sufficient collector current to produce saturation if that occurs.

A not-too-rough estimate of the discharge time may be made as follows:

1) The base current is approximately 10/22 ma, and the collector current for the unsaturated transistor is approximately β times greater. Use a nominal value of, say, β=100 to estimate the peak current to be 55 ma. The saturated collector current is approximately 10/2.2 ≈ 4.5 ma. Assume as a rough approximation to the actual circumstances that the capacitor is discharged by a constant current which is the average of the two extreme values, i.e., by 30 ma.

2) The collector voltage change is a bit less than 10 volts.

3) Replace differentials by finite differences in the volt-ampere relation for a capacitor to estimate Δt = CΔV/I = 1 µf x10 v /30 ma = 0.33 millisecond

Compare this estimate of the fall time with what the oscilloscope display shows.

**Astable Multivibrator**

Suppose two copies of the switching circuit used in the preceding experiment are cascaded, with the output of the cascade brought back to the input; the circuit is illustrated to the right. However, for the moment, imagine that the output-to-input connection is broken at A-A, and a square wave input is applied through the coupling capacitor to T1. For the first stage this is the same situation as in the preceding experiment, and hence a rectangular waveform is generated at the T1 collector. (Actually the loading by the coupling capacitor to T2 causes a finite rise time.) The pulse input to T2 from the T1 collector provides the same triggering action as the input to T1, and so a rectangular waveform appears at the collector of T2. This behavior is easily verified experimentally.

It is also not difficult to verify that the waveform taken from the collector of T2 has the proper timing to be applied to the input of T1 to maintain the switching of both stages. This relationship also may be inferred by redrawing the circuit in the symmetrical fashion shown in Fig. 20-4. It also can
be verified directly by reconnecting the feedback connection (first remove the external input) to form a 'ring'. There is a philosophical question here; where does the first pulse come from to start the oscillation. In general the circuit is 'self-starting', i.e., inevitable asymmetries and thermal noise will cause one of the stages to trigger the other immediately the output-to-input connection is completed.

This circuit is an example of a 'relaxation' oscillator. Each stage can operate in either of two states, one with the transistor saturated and the other with the transistor cutoff. However the cutoff state is metastable, i.e., it has a finite duration determined by the recharging of the base capacitor. The two stages are connected so that as one stage 'times out' of its metastable state it switches the other stage into the metastable state. Once switching is started it persists indefinitely.

Experiment # 20.2
Assemble the relaxation oscillator circuit and observe the waveforms. Compare measured waveform amplitudes and timing with calculated values. Note that the supply voltage is changed to +5 volts for this circuit. The reason for this is that the transistor base-emitter junctions have a reverse-bias breakdown voltage of roughly 6 to 8 volts. The amplitude of the collector voltage change which is applied to the base is about $V_{cc}$. Limiting the supply voltage avoids the breakdown. While the breakdown is not destructive unless excessive currents are involved, it obscures the basic circuit operation without any particular advantages. (If you wish raise the supply voltage to +10 volts and display the base voltage. When the junction breaks down it holds the base voltage substantially constant, but increasing slowly as the capacitor charges. Eventually the junction voltage increases to a point where recovers its reverse-bias blocking capability, and thereafter the base voltage rises exponentially as before. The basic effect is to flatten the starting tip of the exponential base voltage rise.

**Totem Pole' Switching**
Charging (or discharging) a capacitor through a series resistor introduces 'extra' delay because the change in voltage across the capacitor changes the voltage across the resistor, and that change affects the current adversely insofar as the charging is concerned. Or, if you prefer, the circuit time constant is larger the larger the resistance involved. In the transistor switching circuit for the preceding experiments capacitors loading the collector must be charged through the collector resistor. This creates a classic trade-off conflict. If the collector resistor is made small the saturation current is high, requiring a more robust power supply. If the resistor is large the circuit time constant is larger slowing the charging. This conflict is resolved in some applications (for example, in T2L logic circuits) by replacing the collector resistor by an 'active' load, i.e., by a transistor. The load transistor acts as a nonlinear resistance, limiting the steady-state current but capable of sourcing a large charging current. A circuit arrangement similar to that used in the T2L family of logic circuits, referred to as a 'totem pole', is shown in Fig. 20-5 below.

The T1 transistor provides out of phase voltages to drive the totem pole formed by T2 and T3. If T1 is cut-off the collector and emitter voltages of T1 are such as to turn T2 on and T3 off concurrently; vice versa if T1 is on and saturated. (The diode at the emitter of T3 is used to assure that the saturated collector voltage of T1 does not turn on T3 when T2
is saturated.) When T3 is on (and saturated) it provides effectively a low resistance connection to the
supply through which the load capacitor can be charged more quickly. The 100 Ω collector resistance is a
current-limiting resistor added for short-circuit output protection.

Experiment #20.3 (OPTIONAL)
Assemble the totem pole circuit as shown, except initially substitute a 2.2 kΩ resistor for T2. Observe the
collector voltage of T2, noting the rise and fall times. Then replace the 2.2 kΩ resistor by the active load
T2, and note the rise and fall times in the changed circuit. Compare the two sets of observations.

'Bootstrap' Voltage Ramp Generator
Although not entirely a matter of capacitive switching the following topic is of some interest on its own
merits; since it involves a capacitor and switching it is included here. The circuit diagram below illustrates a
'bootstrap' ramp generator, used to obtain a near-constant rate of change of voltage. The basic arrangement
for producing the ramp voltage is the RC charging circuit. The square wave applied to the transistor base
switches that device between saturation and cut-off. In the saturated condition the capacitor C is
discharged, and in the cut-off condition the capacitor is
charged through the resistor R. (The duration of the
cut-off condition is assumed to be long enough for
the capacitor to charge fully.)

However the charging current in a simple RC circuit
is exponential, and the exponential is approximately
linear only initially, i.e., for a time short with respect
to the circuit time constant.

The exponential waveform comes about because as
the capacitor C charges the voltage drop across the
charging resistor R decreases. Hence the charging
current, which flows through that
resistance, decreases and consequently the rate of charging also decreases. A linear voltage rise requires a
constant charging current to be maintained. The additions made to the basic RC charging circuit attempt to
maintain such a constant charging current by measuring the increase in voltage across the capacitor (or
just the capacitor voltage, assuming the capacitor is uncharged initially), and increasing the voltage at the
upper end of the resistor by the same amount so that the voltage drop across the resistor remains
approximately constant. (The designation 'bootstrap' is a reference to the facetious suggestion that a person
lift himself off the ground by pulling up on his bootstraps.) The bootstrap capacitor C* >> C is chosen
large enough so that it does not discharge very much during the period over which the RC charging occurs;
in this way it acts approximately as a fixed voltage source during this period. Hence as the voltage
follower raises the voltage on one side of C* the other side rises approximately the same amount.
(Because there is a small discharge of C* the compensation is not quite perfect.)

Suppose that initially C is fully charged to VCC, and there is no voltage across C*. To start the charging
cycle the transistor is turned on (saturated) to discharge C rapidly. As the voltage across C drops the
voltage follower sinks current provided by VCC to charge C* through the diode very quickly. The
transistor then is turned off to start the ramp generation. Since C is discharged initially charging current
flows through R, the voltage across C increases, and the voltage follower passes the change along to the
other side of R.

Since C* does not discharge much (by design) as soon as the voltage rises a few tenths of a volt the diode
is reverse biased; this means the power supply cannot supply the current to continue to charge C. The
charging current for C actually is supplied by C* during the charging cycle. As noted above C* is
recharged from VCC at the beginning of each cycle when C is discharged. The
A bootstrap process would continue indefinitely since it is a regenerative feedback condition, except that the amplifier eventually saturates and the voltage follower action stops. In general, the output saturation voltage will be \( \approx V_{cc} \), since this likely will be the amplifier supply voltage.

An equivalent circuit in the transform plane for the bootstrap generator is drawn to the left. A straightforward analysis provides the results:

\[
e(s) = \frac{C^*}{C} V_{cc} \left\{ \frac{1}{s} - \frac{1}{s + \frac{RC^*}{1}} \right\}
\]

\[
e(t) = \frac{C^*}{C} V_{cc} \left\{ 1 - e^{-t/(RC^*)} \right\} \approx V_{cc} \frac{t}{RC^*} \left\{ 1 - \frac{1}{2} \left( \frac{t}{RC^*} \right)^2 \right\} + ...
\]

The equations indicate, as expected, that the charging is done with an effective time constant \( RC^* \gg RC \). Note that the amplifier saturation voltage \( V_{cc} \) is reached in one RC time constant; the series expansion of the exponential provides a measure of the 'error', i.e., the departure from perfect linearity, at that time. A sketch of the ramp waveform is drawn as Fig. 20-6.

**Experiment 20.4:**
Assemble the bootstrap circuit; drive the transistor switch with a square wave from the function generator, adjusting the period to allow the amplifier to saturate before restarting a ramp generating cycle. Compare measured circuit performance with theoretical expectations, particularly the duration and amplitude of the ramp. Replace \( C^* \) by a smaller capacitor (e.g., 1 nf) and report on the change in the waveform generated.

**Inductive switching**
Energy is stored magnetically in an inductor by the work done to establish a current flowing through that inductor. Since energy is conserved this stored energy can neither appear nor disappear spontaneously. Hence if the current flow through the inductor is to be changed a corresponding change in stored energy must occur. As a practical matter work is done at a finite rate, and hence finite changes in energy take a finite time to accomplish; inductor current flow does not change instantaneously. To provide the energy change associated with a changing inductor current a voltage difference across the inductor is induced, reflecting the work involved per unit charge to change the magnetically stored energy. The familiar volt-ampere relation for a linear inductor is

\[
e = L \frac{di}{dt}
\]

where \( i \) is the inductor current, \( e \) is the generated ('induced') voltage, the proportionality constant \( L \) is the inductance, and \( t \) is time.

A principal objective of this part of the experiment is to provide direct experience with and better understanding of circuit aspects of inductive transients. The circuit drawn in Fig. 20-7 is used for this purpose. For the moment, and only for the temporary purpose of this paper discussion, ignore...
the diode/resistor network within the dashed rectangle.

The inductance might be associated with the energizing coil of a relay, a not uncommon context for the circuit shown. Ordinarily the resistance in series with the coil would be only the intrinsic resistance of the inductor winding. However an additional resistance is inserted here to assure collector current-limiting to a safe value and, as an incidental benefit, to provide an indirect means of viewing collector current.

Suppose, initially, that the transistor is cutoff, i.e., no current flows through the coil and therefore there is no magnetic energy stored in the inductor. This steady-state condition then is changed abruptly by turning the transistor on with a positive-going base pulse. (Zero DC voltage offset is assumed. The pulse width is assumed to be wide enough so that steady-state conditions are reestablished between pulse edges in order that essentially independent turn-on and turn-off transients can be viewed concurrently.) The transistor itself responds much faster than the inductive changes and so turns on essentially immediately when the emitter junction is forward-biased. However the magnetic energy stored in the coil cannot change instantaneously, and so the coil current, i.e., the collector current, must remain zero initially. An ON transistor (emitter junction forward-biased) and a zero collector current are compatible only in the saturation region of the collector characteristic near the origin. (The CE characteristic curves pass though zero current when the collector-emitter voltage is very slightly positive.) Hence to satisfy KVL, KCL, and the volt-ampere relations of the various circuit elements the collector voltage drops to a near-zero value initially. The drop is supported by a voltage induced in the coil by the changing current. Although the initial current is zero the initial rate of change of current is not zero. Rather the initial rate of change of current is whatever it needs to be to provide the voltage drop necessary to lower the collector voltage to the point of zero collector current. Thus the transistor turn-on, as interpreted on the collector characteristics, starts with the operating point at zero current and a collector voltage of Vcc (transistor cutoff condition) and then moves over more or less instantaneously to zero current and a very small collector voltage. Thereafter the transistor operating point moves along a constant base current characteristic (corresponding to the constant base drive applied) until a new steady-state condition is reached. Ordinarily the steady-state operating condition would be designed so the transistor is saturated (as in the circuit shown), i.e., below the knee of the collector characteristic. There is no particular benefit to dissipating energy gratuitously in the transistor, so ordinarily it would be operated at the lowest collector voltage and base drive that provided sufficient collector current to energize the relay coil reliably.

The turn-on transient generally is fairly fast; the turn-on time can be estimated for the given coil inductance by approximating the saturation part of the collector characteristic with a PWL equivalent circuit. An adequate approximation is a resistor whose resistance would be of the order of 1 volt (= saturation voltage) divided by currents of the order of a few tens of milliamperes or less, i.e., a few hundred ohms. This 'resistor' is in series with the coil inductance and resistance; the latter probably will have the larger resistance. The time for the current to rise to within one percent or so of the final value would be four or five time constants. The turn-on transient is illustrated as part of the graph of collector voltage vs time drawn below (Fig. 20-8).

Note that the introduction of the temporarily ignored diode branch in the collector circuit would not affect turn-on conditions significantly since the diode would be reverse-biased throughout the transient.

Assume now that the transistor has reached a steady-state (saturated) condition after being turned on, and then it is turned off by removing the base drive. The immediate result, if no precautions are taken, might well be the destruction of the transistor! The reason for this is associated with the energy stored in the
magnetic field of the coil in the course of establishing the collector current flow, energy which can not simply disappear spontaneously. What happens is that the coil current starts to decrease when the base drive is removed, and this change in current induces a voltage across the coil with a polarity that increases the collector voltage. The faster the current change the larger the induced voltage. A fast cut-off of the transistor can cause a correspondingly large induced voltage to appear at the collector.

The increased collector voltage actually tends to maintain collector current flow because of the finite slope of the collector characteristics. Thus as the base current is reduced a bit, tending to reduce the collector current, the collector voltage increases to provide a compensating increase. This action rapidly carries the collector junction into a destructive breakdown condition. Although often not emphasized in describing the collector characteristics it is possible for the collector current to become quite large with little or no external base current drive applied. This anomalous condition occurs when the collector-base junction is sufficiently reverse-biased to begin to enter its avalanche breakdown region. Avalanche generated carriers produced in the collector junction region are injected into the base and so constitute a base current, albeit an internally generated current; the effect of this injection current is similar to base current provided from an external source. Consequences of this internal current actually become significant below the 'knee' of the junction breakdown characteristic because of transistor action, i.e., a small avalanche base current increase is amplified to produce a large collector current increase. For good reason however operation of the transistor in this region is not recommended. The collector dissipation is high since there is substantial collector voltage and current, and the collector current is sensitive to small changes in collector voltage and resultant changes in avalanche generated carriers. In the case of the inductive turn-off the collector voltage increases considerably unless inhibited as the circuit attempts initially to maintain the coil current without external base drive. Almost invariably if precautions are not taken the result is excessive transistor dissipation and virtually instantaneously consequent destruction of the transistor. Since the fundamental physical requirement of energy conservation requires the stored energy to be removed one way or another a controlled (safe) method of removal is necessary to avoid the destruction of the device.

This is the purpose of the 'freewheeling' diode across the inductor branch, which is dormant until the turn-off transient occurs. When the voltage induced by the inductor causes the collector voltage to rise the diode becomes forward-biased, and this provides a current–carrying loop which replaces the current path through the transistor. The stored energy often can be dissipated in the coil resistance alone but an additional resistor may be added in series with the diode as shown to dissipate the stored energy of the coil more quickly.

There is a trade-off involved here. The coil current, which initially is equal to the collector current, flows through the diode-resistor branch when the transistor is cutoff. That determines the initial voltage generated inductively; it is VCC + the diode forward-bias + the voltage drop across the diode-branch resistor. The higher the resistance the larger the power dissipation and the faster the turn-off, but also the larger the initial voltage across the transistor (and the greater the reverse breakdown voltage required for the transistor). The inductive turnoff transient also is shown on the sketch of the collector voltage vs time in Fig. 20-8.

**Experiment #20.5**
For this experiment assemble the inductive circuit shown in Fig. 20-7; include the diode branch and be sure the diode is connected with the proper polarity. Produce an oscilloscope display of the collector voltage transient corresponding to the previous illustration. Concurrently (dual trace) display the base voltage. Describe the relationship between the two displays in your report. Make appropriate measurements and collect data necessary to calculate the turn-off collector voltage jump and decay time. Make the calculations and compare them to measured values. Determine the turn-on delay from the oscilloscope display and compare with an estimate made as described previously; don't forget to account for the collector resistor.

Display the voltage Vi (defined on the circuit diagram) concurrently with either the base drive or the collector voltage. Vi is the saturation voltage of the transistor while it is on, and when the transistor is off Vi tracks the inductive diode current decay. Describe and explain your observations.

**Experiment #20.6 (OPTIONAL)**
The circuit drawn below illustrates an alternate method of dissipating the energy stored in the inductor when the transistor is turned off. The basic idea is the same as before, i.e., as part of the turn-off procedure of the transistor provide a well-defined current path to dissipate the stored energy safely. The Zener voltage should be greater than VCC, so that the Zener diode is not conducting for the steady-state ON condition of the transistor. However when the transistor is turned off the induced voltage across the coil brings the diode into conduction, and this provides a bypass current path to the transistor base. The transistor is kept on temporarily by this new source of base current, with roughly a constant collector voltage (Zener voltage + emitter junction voltage drop) while the stored energy is dissipated.

Assemble and operate this circuit. Observe the collector voltage and the base drive waveforms concurrently. In your report describe and explain your observations.