Objective
The objective of this experiment is a study of switching dynamics in the context of several multivibrator circuits.

Parts List
resistors 3.3 kΩ, 3.9 kΩ, 6.8 kΩ
capacitors 0.1 µf, 0.01 µf
diode 2 of 1N4004
opamp 2 of 741
CMOS quad 2-input NOR 4002
TTL quad 2-input NAND 7400
integrated circuit 'timer' 555

Bistable, Monostable, and Astable Devices
A circuit (or device) which can maintain a steady-state condition indefinitely in either of two distinct states is said to be 'bistable'. If the circuit can persist in one of the two states only temporarily it is said to be 'monostable', and the temporary state is said to be 'metastable'. If the circuit can persist only temporarily in either state it is said to be 'astable'. Circuits of this sort are classified as 'multivibrators', although the terminology is pedagogical, even archaic; commonly used colloquial terminology is substituted in the course of the subsequent discussion.
**Bistable Multivibrator**

The essential circuit configuration of a multivibrator consists of an amplifier with positive feedback, as illustrated in the sketch to the right. A representative graphical analysis of the circuit is shown below. The solid line in the graph represents the (PWL) transfer characteristic of the amplifier. The amplifier is assumed to have greater than unity gain in its amplifying range, i.e., the slope of the center segment is greater than 1. Ordinarily it would be much greater than 1.

![Fig. 50-1 Amplifier with positive feedback](image)

Although it need not actually be so assume for simplicity that the feedback is linear. Then a plot of the relationship between $V_{in}$ and $V_{out}$ imposed by regenerative feedback is a line with positive slope; a representative line is shown on the graph.

Suppose that the feedback applied is such that there are three interception points; the simplest case for this is a direct connection between input and output, for which $V_{out} = V_{in}$. The feedback plot for this requirement is a line through the origin, and since the slope of the line is 1 it must intersect the amplifier characteristic in three points. The three interception points mark conditions for which the requirements imposed on the circuit both by the feedback and by the amplifier are satisfied concurrently, and represent possible operating points for the circuit.

![Fig. 50-2 Bistable Multivibrator analysis](image)

Two of the interception points correspond to stable operating points; these are the intercepts in the amplifier saturation range. Once placed in either of these two states the circuit is able to operate in that state indefinitely. Moreover after the cause (whatever) of a small perturbation from a stable operating point is removed the circuit resumes operation at the point. Note however that the existence of two stable states necessarily implies a limited range of stability for each state, i.e., given operation initially in one stable state it should be possible to perturb the system sufficiently strongly to force it out of the range of stability for one state and into that for the other stable state. For example if the amplifier happens to be in positive saturation ($V_{out} > 0$) a voltage pulse applied temporarily across the amplifier input can force the amplifier into negative saturation, in which condition it then can remain indefinitely. From this it may be inferred that there is a fragile circuit condition intermediate to the two stable states which is, so to speak, on the borderline between the range of the two stable states. This metastable condition corresponds to the third interception point located in the active gain region of the amplifier.

![Fig. 50-3 Metastable operating point](image)

The figure to the right shows a portion of the preceding figure. Suppose the amplifier happens to be saturated positively when a perturbation of some sort forces the input voltage to lesser but still positive value $V^*$ (greater than the value corresponding to the metastable point) in the active gain region. The amplifier output then is greater than $V^*$ (amplifier gain greater than 1). But the feedback requires $V_{in} = V_{out}$ (change indicated by the horizontal dotted line); amplification then increases $V_{out}$ (vertical
dotted line). This regenerative action continues until the circuit stabilizes at the intercept in the positive saturation region. This ability to recover from a perturbation of limited extent is the essential attribute of a stable state.

However if the perturbation had carried the operating point beyond the origin, i.e., beyond the metastable state, the regenerative action would move the amplifier all the way to the negative stable intercept. The metastable intercept itself has a very delicate theoretical stability; the slightest perturbation from the metastable state is exacerbated continually until the operating point rests at the saturation intercept toward which the perturbation first headed. A perturbation of some sort, e.g., thermal noise, is a practical inevitability and operation in practice would be at one or the other stable point.

The canonical name for a circuit exhibiting two stable operating points is 'bistable multivibrator'. Modern colloquial terminology generally calls such a circuit a 'flipflop' (or, in certain instances, a 'latch'). Such devices are widely used in digital logic circuits, and complete functional devices are available inexpensively in integrated circuit form. A 'latch' assembled with NAND gates is illustrated to the left. The upper circuit clearly shows the feedback constraint $V_{\text{in}} = V_{\text{out}}$. The inputs labeled 'trigger' are used to apply controlled 'perturbations' to force the operating point to switch from one stable condition to the other. The lower circuit is topologically identical to the upper circuit; it is reconfigured merely to emphasize the symmetry of the circuit shown.

**Monostable Multivibrator**

It should not diminish the importance of the flipflop to note that a modification of the bistable condition is of more interest for this particular experiment. As illustrated in the figure below the feedback constraint is modified (in a manner illustrated later) so that there is a single intercept point. Both of two closely related possibilities are illustrated in this figure; the interception point could be in one or the other of the saturation ranges of the amplifier. In either case the interception point provides a single stable operating point.

Historically a circuit with a single stable operating point is called a monostable multivibrator. The modern colloquialism is 'one-shot', for reasons that will emerge in the discussion. The one-shot as described thus far becomes a useful device with the addition of two control capabilities. One is the addition of explicit means for momentarily forcing the operating point away from stable operation. Of course when this 'perturbation' is removed the circuit returns to operation at the solitary stable operating point.
The second control addition is an arrangement of some sort which delays the return to operation at the stable intercept for a fixed period of time. The resulting circuit is one which can be forced into a metastable state, and remains there temporarily for a prescribed lifetime. The beginning and end of this metastable state then provide timing marks which can be used in several ways. For example, suppose an event that occurs at unpredictable intervals of time requires a responsive action to be taken a fixed time after each occurrence. A trigger signal generated by the first event can initiate the metastable state of a one-shot. The exit from the metastable state a fixed time later then provides the timing mark for the second action.

A representative one-shot circuit is drawn below, including a sketch of the voltage waveform at the amplifier inverting input when the circuit is triggered. The amplifier is assumed to saturate at ±$V_{sat}$ respectively. The input to the trigger diode $D_1$ simply ‘floats’ when there is no trigger signal, and the circuit is designed to make the voltage division ratio $\beta$ such that $\beta V_{sat} > 0.7$ volt, i.e., to forward-bias the diode $D_2$. This forces the stable state of the amplifier to be $V_{out} = +V_{sat}$. (Why?) The resistor $R$ should be large enough to limit the $D_2$ diode current to an acceptable value. The steady-state condition is shown on the left side of the plot of the voltage at the inverting input vs time.

To trigger the one-shot a negative pulse coupled through the $D_1$ diode (momentarily forward-biasing $D_1$) forces the voltage at the noninverting input below that of the inverting input to rapidly switch the output voltage to $V_{out} = -V_{sat}$. The trigger pulse duration should be less than the duration of the metastable state that it initiates; the pulse ‘clamps’ the voltage at the noninverting input, not allowing this voltage to be set by the voltage divider action.

By reversing the polarity of the input voltage the amplifier output switches to $-V_{sat}$, and assuming a large amplifier gain the threshold voltage at the noninverting input becomes $-\beta V_{sat}$ (when the trigger pulse is withdrawn). The reversal of output voltage polarity reverse-biases the diode $D_2$ at the inverting input, permitting the capacitor to charge exponentially from an initial +0.7 volt toward $-V_{sat}$ with a time constant $RC$; this is shown in the transient plot also.

As long as the voltage at the inverting input remains less than the threshold at the noninverting input, which is $-\beta V_{sat}$, the amplifier output remains at $-V_{sat}$. Eventually however the decreasing (towards $-V_{sat}$) voltage at the inverting input necessarily becomes less than the voltage at the noninverting input, and the amplifier output switches back regeneratively to $V_{sat}$. Note however that the voltage at the inverting input is not restored to its steady-state value immediately. Instead the capacitor charges exponentially toward $+V_{sat}$ until the diode at the inverting input becomes forward-biased and clamps the voltage.

**Experiment # 50.1**
Assemble a one-shot circuit configured as illustrated above. Use (nominal values) $R=10k\Omega$ and $C=0.1\mu f$. Use a 10 k$\Omega$ potentiometer as the voltage divider for the positive feedback so that the value of $\beta$ can be varied. Sketch, using a common time scale, both the voltage at the inverting input and the amplifier output voltage as observed with the oscilloscope. Explain how the metastable state is maintained. Why should
the trigger pulse width be less than the metastable state period? Make the appropriate measurements to determine the period of the metastable state and compare with calculated values. Observe, describe, and explain what happens to the amplifier output waveform as \( ß \) is varied between 0 and 1.

Note: Depending on the function generator used it may be difficult to make the square wave pulse period small compared to the metastable state duration in a direct fashion. To overcome this problem differentiate the square wave to get short pulses (ideally impulses). The RC voltage divider illustrated to the right is used for this purpose.

Make the reactance of the capacitor large compared to the resistance for a nominal repetition frequency. Then the current through \( C \) and \( R \) is essentially proportional to the derivative of the input voltage train, and the voltage across the resistor is proportional to this derivative. The negative 'spikes' so produced provide short duration trigger pulses. Note that a positive pulse need not be 'clipped' (with a diode) to remove it since the amplifier is saturated when it occurs.

**Alternate 'One-Shot' Configuration**

An alternate one-shot configuration is shown below. The steady-state condition is designed to have the amplifier output voltage equal \(+V_{sat}\). (Ordinarily \( V_{cc} \approx V_{sat} \).) The switching threshold at the inverting input is set to \(+ßV_{sat}\) by the voltage divider. The metastable state is triggered by dropping the trigger voltage momentarily, forcing the amplifier output to switch to \(-V_{sat}\). Note that the switching threshold voltage at the inverting input drops concurrently to \(-ßV_{sat}\).

The capacitor begins to charge towards \( V_{CC} \), but initially the voltage across the capacitor does not change. Since the voltage at the output side of the capacitor has dropped by \( 2V_{sat} \) so also does the voltage at the noninverting input. The amplifier remains in the metastable state until the capacitor charges sufficiently to reverse the input voltage, and then the output voltage switches regeneratively back to \(+V_{sat}\). As before the voltage across the capacitor cannot change instantaneously, and so the noninverting input voltage is pulled up at first, and then it decays exponentially towards \( V_{CC} \) to restore the steady-state. The one-shot transient is drawn to the right of the circuit diagram.
**Experiment # 50.2 (OPTIONAL)**

Assemble the alternate one-shot circuit configured as illustrated above. Use (nominal values) $R=10\, \text{k}\Omega$ and $C=0.1\, \mu\text{F}$. Use a 10 kΩ potentiometer for the resistive divider so that the value for $\beta$ can be varied. Relate the voltage at the noninverting input and the amplifier output voltage as observed with the oscilloscope. Where is the regenerative feedback? Why should the trigger pulse width be less than the metastable state period? Make the appropriate measurements to determine the period of the metastable state and compare with calculated values. Observe, describe, and explain what happens as $\beta$ is varied between 0 and 1.

Note: Use the RC trigger circuit described before if necessary.

**IC 'Timer'

The '555' integrated circuit is designed specifically to implement a relaxation process; the circuit below illustrates both the ideas underlying the '555' and its use in implementing a one-shot.

![IC 'Timer' Circuit Diagram](image)

**Fig. 50-9 Integrated circuit 555 'timer'

The '555' configuration is shown inside the heavy lines and consists of a resistive voltage divider, two comparators, a flipflop (with an output driver), and a transistor switch. The monolithic technology with which the chip is assembled produces well-matched resistor values, so that the voltage taps correspond to a well-defined voltage ratio. As will be seen it is a voltage ratio rather than the absolute voltage that is the more important parameter.

The flipflop provides two stabile states, with the Set-Reset inputs triggering a switch from one state to the other. It is initialized to $Q = \text{logical 0}$ by the asynchronous reset control, and this forces the device output to 0 volts. Concurrently the transistor is turned on (saturated) and discharges the capacitor rapidly. The output of comparator #1 goes low, applying a logical 0 to the R flipflop input. The inactive state of the Trigger input voltage is above $V_{cc}/3$, so that the output of comparator #2 is low, corresponding to a logical 0 at the S input of the flipflop.

To initiate a change of state the trigger input is brought below $V_{cc}/3$ briefly, 'setting' the flipflop, and then is restored to its inactive state. The change in state forces the device output high, and cuts off the transistor to allow C to charge towards $V_{cc}$. But when $C$ charges to $2V_{cc}/3$ the flipflop R input is triggered to restore the original state. The temporary state persists while $C$ charges exponentially from approximately zero (saturated transistor) to $2V_{cc}/3$ with time constant $RC$. A straightforward calculation obtains the expression one-shot period $= RC \ln 3 = 1.1 \, RC$. 


Experiment # 50.3
The circuit diagram of a one-shot assembled from a 555 timing IC (pinouts shown are for the eight pin DIP) is drawn on the preceding page. Assemble the circuit, and measure the period of the metastable state. Compare this with the calculated value.

CMOS One-Shot
Logic gates can be used to assemble a one-shot; an illustration using CMOS NOR (4002) gates is shown. For the present purpose the NOR gate may best be regarded as a high-gain inverting amplifier designed for either saturated or cutoff operation, and equipped with triggering inputs used to switch between these states. In the steady-state condition (trigger low) gate #2 output is low and gate #1 output is high. When a trigger pulse (logical 1, amplitude >Vdd/2) is applied the gate #1 output is forced low concomitantly lowering the input to gate #2 and forcing its output high. This metastable state is maintained until C, charging exponentially through R, reaches the logical 1 voltage level and switches the gates regeneratively back to the stable state.

Waveforms at the circuit points indicated are drawn to the left. The waveforms are similar to those drawn for one of the one-shots described earlier, except that some internal CMOS gate circuit components have an observable effect. Most CMOS circuits have internal protection diodes connected from Vdd to each gate input, and from each gate input to ground. These diodes, normally reverse-biased, protect against voltage surges.

The regenerative switching of gate #1 ordinarily would pull Vb well above Vdd temporarily, but breakdown of a protection diode clips the rise as shown. It also provides a current path that clips the voltage rise of Va also. Vc is insulated from these effects and displays the intrinsic gate output switching characteristic.

Experiment # 50.4
Use a quad 2-input CMOS NOR IC to assemble a one-shot as described, and verify the waveforms illustrated. Use R = 10 KΩ and C= 0.1 µf.

Astable Multivibrator
For an astable multivibrator, commonly called a 'clock' or a 'relaxation oscillator', both circuit states are metastable, and there is continual switching from one state to another (with an extended persistence in each state before switching to the other state). Continual switching of this sort can be obtained with two one-shots interconnected so that the termination of the metastable state in one of them initiates the metastable state of the other.
To illustrate this first consider the simple one-shot illustrated to the right. In the absence of an input voltage the amplifier output will be the negative saturation voltage; the diode is forward biased through the resistor.

If a rising step voltage is applied the capacitior charges quickly through the forward-biased diode to the pulse height; the amplifier remains saturated during this charging.

On the falling edge of the pulse the diode is reverse-biased, and the capacitor must recharge through R with a time constant much larger than the input pulse fall time. Hence the voltage across the capacitor is unchanged initially, and the noninverting input voltage drops quickly and reverse-biases the diode. This forces the amplifier output voltage to switch to into positive saturation, where it remains temporarily as the noninverting input voltage charges toward Vcc.

The amplifier output recovers when the noninverting input voltage turns the diode on again. The waveform at the noninverting input is illustrated to the right.

The output voltage of the amplifier is a pulse, and that pulse can be used to drive a second one-shot stage (which need not have the same time constant as the first). Similarly the output of the second one-shot can be used to drive a third one-shot. In fact the pulse timing is such that the second stage can supply the pulse for the first stage, i.e., the two stages can drive each other in succession indefinitely to form an astable multivibrator (clock). Of course an initial pulse must be supplied to start the process but as a practical matter thermal noise and circuit asymmetries (element tolerances for example) assure an automatic starting pulse when the circuit is first activated.

**Experiment # 50.5**
Assemble the clock circuit discussed. Design for a period of ≈ 0.1 millisecond, with a 2/3 duty cycle (the pulse period for one amplifier output is twice that of the other). Open the feedback connection and externally trigger the one-shot of the left; verify your pulse period computations for both one shots. Reconnect the feedback. Verify astable operation, comparing the observed waveform to that calculated. Compare the pulse trains at the two amplifier outputs. Explain your observations in the report.
Another Clock
A related approach to a relaxation oscillator is illustrated by the circuit drawn to the right. This circuit is the same as that of a one-shot considered earlier, except that the diode across the capacitor is replaced by a resistor. Recall that the diode was used to establish the monostable state by 'short-circuiting' the capacitor. The voltage divider at the top of the amplifier is used to set a regenerative switching threshold at the noninverting input as before. However the actual threshold voltage that is set depends on the output voltage, i.e., on which saturated state the amplifier is in.

Assume, for the sake of argument, that the current metastable state of the amplifier is \( V_{\text{out}} = +V_{\text{sat}} \). This state requires that the voltage at the noninverting input be greater than that at the inverting input. However such a condition can be at best only be a temporary one in the circuit shown. The voltage toward which the capacitor charges is \( kV_{\text{sat}} \), and the constraint placed on the value of \( k \) means this voltage is larger than the noninverting input voltage. Eventually therefore the capacitor will charge to a voltage at which the amplifier input will reverse polarity, and the output will switch states regeneratively. (In the one-shot circuit the diode clips the rise before the threshold is crossed.)

A similar metastability occurs if the amplifier output initially is in the state opposite to that assumed above. In other words whichever the saturated state the amplifier is in initially it will after some time relax (i.e. switch) to the other saturated state.

The time spent in each metastable state, and so the period and duty factor of the oscillation, depends on how far the capacitor must charge or discharge between its voltage level on first switching into a metastable state, and the switching threshold. A graph of the voltage waveform at the inverting input is shown below. A critical point to note is the placement of a switching threshold for a given output state between the value of the voltage when the state is initiated and the final voltage towards which the capacitor heads, insuring that the switching threshold will be crossed.

Experiment # 50.6
Design a relaxation oscillator of the alternate form illustrated above for a nominal 1 kilohertz repetition rate. Use a potentiometer to obtain a variable 'k' capability. Assemble your circuit and compare measured values of amplitude and time to your design calculations. Observe the effect of varying 'k'; explain your observations.
Alternate Relaxation Oscillator Configuration (OPTIONAL)

In the preceding circuit configuration the capacitor is charged while in a given state until the switching threshold is reached. That is, the capacitor accumulates charge until enough energy is stored to enable switching to the other state. An alternative circuit configuration, illustrated to the right, has the timing capacitance discharged rather than charged, in order to reach the switching threshold. A suitable switching threshold is set at the inverting input; the threshold voltage is different for the two saturated amplifier operating conditions. As will be seen the reference voltage $V_0$ must chosen so that $-\beta V_{\text{sat}} \leq V_0 \leq +\beta V_{\text{sat}}$ for astable operation.

Suppose, for example, that the amplifier output is $+V_{\text{sat}}$, with the threshold for switching at the inverting input then being $\beta V_{\text{sat}}$. For consistency with the assumption about the amplifier output the noninverting input voltage must be greater than $\beta V_{\text{sat}}$, but the circuit also indicates that this voltage is decreasing exponentially towards $V_0$ with time constant $RC$. Because of the condition placed on $V_0$ the switching threshold necessarily is reached and the amplifier output switches regeneratively to $-V_{\text{sat}}$.

Note that the voltage across the capacitor cannot change 'instantaneously', and as the amplifier output voltage drops by $2V_{\text{sat}}$ so does the voltage at the inverting input. This carries the voltage at the noninverting input well below the revised threshold voltage set at the inverting input by the change of state.

Since the voltage at the noninverting input is rising exponentially towards $V_0$ the threshold necessarily is reached, and the cycle repeats. A sketch of the voltage waveform at the inverting input is shown below.

Experiment 50.7 (OPTIONAL)

Yet another relaxation oscillator of the type described above can be assembled with CMOS NOR gates as illustrated to the right. The CMOS gate (4002) output switches between saturated states with outputs of zero (essentially) and $+5$ volts respectively; the switching threshold is 2.5 volts. In the preceding illustration the oscillation requirement is that the reference voltage $V_0$ lie between the two threshold voltages. Although this constraint achieves the purpose the actual requirement is that the timing voltage change in such a way as eventually to cross the switching threshold. The two-stage character of the logic gate circuit enables this end to be achieved somewhat differently. Thus when gate #1 switches state it pulls the voltage at the input of gate #1 to one side of the switching threshold, while the output voltage of gate #2 is on the other side of the threshold. Hence as $C$ charges the switching threshold will be crossed, assuring astability.
An improvement in operation is obtained by inserting a large resistor $r$ in series with gate #1 to isolate the timing components from the effect of 'protection' diodes built into the CMOS gate. The normal gate input resistance is high so the resistor doesn’t affect the gate operation. Nominally $r \geq 10R$.

Assemble a CMOS astable multivibrator with a nominal repetition rate of a few kilohertz, observe the timing and output waveforms, and describe and explain these for your report.

**Experiment 50.8 (OPTIONAL)**

The circuit diagram below is that of a ‘555’ timer integrated circuit operated as an astable multivibrator. The timing capacitor charges to $2V_{cc}/3$ through the series combination of the 3.9 and 3.3 kΩ resistors, and discharges to $V_{cc}/3$ through the 3.3 kΩ resistor.

Assemble the circuit and observe the waveforms. Compare the observed period and duty cycle with calculated values.

![555 timer connected for astable operation](image)

*Fig. 50-21  555 timer connected for astable operation*