Diode Modulator (switch)
The sizeable difference between forward-bias and reverse-bias conduction of a diode is suggestive of the open-closed states of an electrical switch, and forms a basis for the (simplified) electronic switch circuit illustration to the right. A signal source \((V1 – R1; V1 \geq 0)\) is connected through a diode network D1-D2 to a load \(R2\). The control voltage \(VC\) is a rectangular pulse waveform with amplitude greater than the maximum of \(V1\). During the pulse time \(D2\) is reverse biased and the source signal is passed to the load through the effective low resistance of a forward biased diode. Absent the pulse the control voltage ‘pulls’ the base of \(D2\) down to ground (and so also the anode of \(D1\)) effectively inserting a high resistance (reverse-biased diode) in series with the load.

For a specific illustration assume (refer to the circuit diagram above) \(R1 = 1\, \text{k}\Omega, R2 = 4.7\, \text{k}\Omega\). Make \(VC\) a square wave of amplitude 5V with a nominal duty factor of \(1/3\) (\(TR = TF = 5\, \mu\text{second}, \text{PW} = 40\, \mu\text{seconds}, \text{PER} = 100\, \mu\text{seconds}\)), and use the 2N4148 PSpice switching diode model. For purposes of illustration \(VS\) is a triangular waveform of amplitude 4V and a period of 2 milliseconds. PSpice data is plotted below.

To estimate circuit performance use a simplified diode model comprising an open-circuit for reverse bias, and a fixed junction voltage \(VD = 0.7\, \text{V}\) source for forward bias. Thus when \(D2\) is reverse
biased estimate the output voltage as

\[ V_o = \left( V_S - V_D \right) \frac{R_2}{R_1 + R_2} \approx (V_S - 0.7)(0.82) \]

This estimate also is plotted above. Other comparisons between the computed and predicted data are left as an exercise.

‘Balanced’ Diode Modulator

In the preceding diode switch circuit the junction voltage drop of the ‘switch’ diode appears in the output voltage expression. This annoyance is removed (largely) with the introduction of an additional diode oriented as illustrated on the right.

It would be hasty but not be unusual to question how back-to-back diodes D1 and D2 can be used to effect a connection between the source and the load. Understanding can begin with the appreciation that the diodes really are not in a simple back-to-back connection; there is the additional current path provided by the control branch connection to consider. For a sufficiently positive control voltage both diodes D1 and D2 can be placed in forward bias concurrently. In this circumstance the source V1 can (and does) moderate the current through D1, and Kirchoff’s Current Law cause associated changes in the current through D2. Thus while there may not be a direct current path through the diodes there is a coupling between the two currents.

To estimate the output voltage Vo (when both diodes are forward biased) model the diodes as fixed voltage sources of strength VD. Estimate (try superposition) the output voltage as

\[ V_o = \frac{V_S - V_D}{1 + \frac{R_1}{R_2|R_3}} + \frac{V_C}{1 + \frac{R_2}{R_1|R_3}} + \frac{V_D}{1 + \frac{R_1|R_2}{R_3}} \]

It is appropriate to emphasize again that this expression is applicable provided VC > VS, or more precisely when the control pulse forward biases both diodes.

Suppose resistance values are chosen as follows:
- a) R1<<R2||R3, so that the denominator of the first term is approximately 1;
- b) R2 >> R1||R3, so as to de-emphasize the contribution of the second term;
- c) R3 >> R1|R2, so that the denominator of the third term is approximately 1, and will cancel (approximately) the VD in the first term;

Under these conditions Vo \( \approx \) VS. For a specific illustration assume R1 = 1kΩ, R2 = R3 = 47kΩ, and determine that

\[ V_o = \frac{V_S - V_D}{1.042} + \frac{V_C}{49} + \frac{V_D}{1.021} \approx V_S \]

Note again that this voltage estimate is valid only during the interval when the control pulse places the diodes into forward bias.
Make VC a square wave of amplitude 10V (TR = TF = 5µsecond, PW = 40 µseconds, PER = 150 µseconds), and use PSpice diode models. For purposes of illustration assume VS is a triangular waveform of amplitude 4V and a period of 2 milliseconds.

Computed output data is plotted below, along with a plot of the estimated output expression. Comparisons between the computed and predicted data are left as an exercise.

\[ V_o = \frac{V_S}{4} \]

Doubly Balanced Diode Modulator

The diode modulator circuit drawn to the right enables a some performance enhancements. A complementary control voltage (-VC) branch has been added to allow for modulating negative as well as positive source signals. In addition symmetry has been imposed on the circuit assuring (to the extent corresponding components are identical) there is no net control voltage coupled to the output. Further there is no net diode junction voltage drop coupled to the output.

Indeed the output voltage is simply related (apply superposition to verify) to the source voltage:

\[ V_o = \frac{V_S}{4} \]

Data computed using PSpice is plotted below.
BJT Analog Switch
It is not difficult to imagine the two diodes in the balanced modulator illustration described earlier to be replaced by a transistor operated alternately between cutoff and saturation. The circuit drawn to the right is the same as the earlier circuit, except for the replacement of the diodes by a BJT and the increase of the R2 resistance to take advantage of the BJT current amplification.

Computed output data is plotted below. Comparisons between the computed and predicted data are left as an exercise.