OPERATION AMPLIFIER (VIRTUAL) PERFORMANCE

The canonical ‘definition’ of an operational amplifier describes it as a high gain voltage amplifier, with high input resistance and low output resistance. This description is idealized to ‘infinite’ gain, ‘infinite’ input resistance, and ‘zero’ output resistance. Instructional exercises, particularly in introductory courses, usually are tailored for operating circumstances in which these approximations are quite good. In practice however this tailoring is not always feasible, and the operational amplifier is an important enough device to warrant a better appreciation of actual rather than idealized operation.

In this note a number of virtual experiments are performed to partially examine the operation of a 741 operational amplifier, an aged but nevertheless still venerable industry standard. Examination of the manufacturer’s data sheet for the 741 make it clear that only a small number of specifications is considered here.

Note: Computer device models in general are rarely a representation of the physical processes underlying the device operation. Mostly they are analog behavioral models, i.e., constructed to mimic typical device behavior. Hence computer computations to ‘measure’ device characteristics are circular in nature; at best they only verify the fidelity of the model to the defining specifications. On the other hand for instructional purposes such computations are useful for familiarization with device performance; a degree of circular reasoning can be tolerated.

Additionally it exercises the use of computer computations to evaluate circuit performance.

DC Transfer Characteristic/Offset Voltage & Current

The test circuit is illustrated to the right. (Sources V4 and V5, effectively short circuits, are added as a convenience; PSpice will automatically record the computed current through voltage sources.) Transfer computations are plotted below.

The amplifier saturates at ±14.4V; a few tenths volt below the rail voltages. This constraint corresponds essentially to saturation of one or the other transistor in the push-pull output stage of the amplifier.

The computed ‘gain’ (upper curve) is 196K (≈106DB). The input voltage change expected for a nominal ±15V output voltage change is about ±15/196K = ±76µvolt as computed.
Incidentally this input voltage difference provides a measure for the conditions under which the idealization of ‘zero’ input voltage is applicable. Thus it is applicable in circumstances where the amplifier input voltage is a negligible term compared to other voltages that would be involved in a Kirchoff loop equation.

Note however that the output voltage is not zero for zero input voltage, or in a more usual description an input terminal voltage of about –20µvolt must be applied to obtain zero output. This voltage offset is a result of manufacturing tolerances and internal device asymmetries.

Note: Although they are not included in the PSpice model the 741 provides externally available pin connections to the emitters of the input differential amplifier stage. The center tap of a potentiometer connected between these terminals can be connected to the negative rail. Varying the potentiometer set point then adjusts the voltage between each emitter and ground, imposing an offset voltage to compensate for the inherent offset voltage.

The final computation made is of the input currents; as can be seen the input resistance is not really ‘infinite’! These currents (for the 741) are the base currents for the differential emitter follower input stage of the amplifier. The currents are not large, but whether they are significant or not depends on the performance requirements of the circuit using the amplifier. In general the appropriate criterion is to compare the input current to other currents in a Kirchoff Current equation at an input node.

The average of the two input currents is the ‘input bias current’.

**Frequency Response**

The 741 OpAmp is internally ‘compensated’, i.e. a capacitor is shunted across the internal gain stage of the, providing negative feedback to establish a dominant pole for the frequency response. This pole considerably reduces the likelihood of spurious oscillation. The incremental-signal frequency response computed by PSpice is plotted below; both amplitude (in DB) and phase shift (in °) are plotted. The theoretical amplitude expression for a single-pole response is superimposed for comparison (using the computed low-frequency gain of 106 DB and a 3DB frequency of 5 Hz).

The gain-bandwidth product is determined from the unity-gain intercept as 1 MHz. Note that the phase shift at the 3DB frequency is –45°, as expected for a dominant-pole response.
Pulse Response

The complement to measurement of amplifier response in the frequency domain is measurement in the time domain, specifically the step function response. However there are practical complications not often described in an introductory examination of operational amplifiers.

As noted before the compensation capacitor is a shunt feedback element across the amplifier internal gain stage, and the output voltage (essentially) appears across this capacitor; an illustrative sketch appears below. To provide the requisite rate of output voltage change a specific input current is required. However the maximum current available to drive the capacitor is limited (there is just so much emitter current in the differential input stage). Hence there is a maximum rate of change of output voltage that can be provided by the amplifier; this maximum is called the ‘slew rate’. For the 741 the typical value for the slew rate indicated by the manufacturer’s specifications is 0.5 volt/µsecond.
To illustrate ‘step’ response a pulse source provides a 1-volt step with a rise time TR of (in turn) 0.1, 0.5, 2, and 10 µseconds. The computed response for the set of steps is drawn below. The response to the step corresponding to a rise time of 10µseconds (0.1 volt/µsecond, i.e. less than the slew rate) is essentially a copy of the input step (except for a small displacement corresponding to the propagation delay through the device)

All the other step inputs involve a rate of change of voltage exceeding the slew rate. The 741 cannot provide this and the rise time of the response for these cases is limited by the maximum slew capability of the device, i.e. 0.5 volt/µsecond.

Incidentally this slew rate limitation is not limited to pulse response. Suppose the output voltage is a sinusoid $V \sin(2\pi ft)$. The rate of change of this output is $2\pi fV \cos(2\pi ft)$, and the slew rate limitation requires $2\pi fV \leq$ slew rate for output fidelity. This leads to the concept of a ‘large signal’ bandwidth, i.e., the frequency at which faithful reproduction of the input fails is lower the higher the output voltage level. The phenomenon is illustrated below for a unit amplitude sinusoid; the slew rate limitation (0.5 volt/µsecond) initiates at a frequency of 79.6kHz.

The first calculation is for a sinusoid of 0.5 volt amplitude; there is no slew rate limitation in this case as comparison with a calculated sinusoid indicates. (There is a small time displacement because of the propagation delay through the device.)

The ‘threshold’ unit amplitude computations are plotted next, and examination indicates the slew rate limitation has some effect. However to make the influence of slew rate explicit a third computation for amplitude 2 is computed. There is no difficulty in recognizing the effect of slew rate in this case.
$V_{\text{out}} = 0.5 \sin(2\pi \times 79.6k \times \text{Time})$

$s\text{lope} = 0.5 \text{ volt/second}$

$V_{\text{out}} = \sin(2\pi \times 79.6k \times \text{Time})$

$V_{\text{out}} = 1.5 \sin(2\pi \times 79.6k \times \text{Time})$