Power Amplifier Project

Introduction
This project involves a modestly sophisticated although not overly complicated electronic amplifier circuit. Specifically it involves a discrete bipolar transistor Class AB output power amplifier using shunt feedback to reduce crossover distortion, and a differential amplifier input stage. There is a modicum of design involved with this project. Design problems typically are ones for which there are fewer independent equations than unknowns, thus requiring both informed judgements as well as specific selections to be made. There is ordinarily not a unique design solution, so that it may be necessary to compare and evaluate alternatives. A few design choices are already made for this specification but others remain to be made.

Not the least part of the design process is the report, conveying clearly, concisely, and accurately what it is you have done. If you can describe what you are doing clearly step by step then you have a considerably improved likelihood of making clear judgements and appropriate design choices. Engineering design is not simply a matter of providing something that ‘works’, whatever that means. A primary thrust of this project is the exercise of an ability to evaluate as well as simply to make choices. Engineering design is a high-stakes game generally intolerant of ‘let’s try it and see if it smokes’ players.

Specification: Power Amplifier Project
Design, test (virtual), evaluate, and report on a power amplifier circuit (see accompanying diagram) to meet performance requirements as described in the discussion following. You should be able, after any circuit element is identified, to explain the function of that element in the circuit and its influence on circuit performance.

Assume the transistors are 2N3904 (NPN) and 2N3906 (PNP) respectively; use nominal device parameter values of $\beta = 120$ and $V_{BE} = 0.7 \text{ v}$. Use a nominal input signal voltage source frequency of 1 kHz. Adjust the input amplitude (suggestion: compute the amplifier gain first) to produce a nominal sinusoidal output voltage of 8v (p-p).

Estimate the performance expected of the amplifier circuit you designed, in particular DC bias voltages and currents, and AC gain. Compare your calculated estimates of DC bias voltages and currents and AC voltage gain against a computer computation using the nonlinear device models. Plot the emitter currents of both Q9 and Q10 on the same axes, and compare to the load (RL) current.

Include explicitly answers to the following questions. How is crossover distortion mitigated? What purpose(s) does R2 serve? How is the DC voltage at the Q9-Q10 emitters determined? Is either Q9 or Q10 (or both) conducting or not in the quiescent state? If either transistor is conducting estimate the emitter current carried and compare to the computed value.

The description of the circuit as given is not entirely complete. Your report should correct for descriptive shortcomings of this discussion without being verbose, e.g. explaining the purpose underlying the inclusion of the various circuit components, e.g., Q6 and Q7.
Notes
There are three functionally distinct sections to the amplifier circuit: an input, an intermediate gain section, and an output section. It is convenient to describe the gain and output sections concurrently.

Q1, Q2, and Q3 form a current mirror to provide bias current to the gain and output stage. The power output stage is a Class AB complementary pair. Shunt feedback provided by R2 is used to reduce crossover distortion.

To the extent the Q8 base current is small compared to the R1, R2 bias the voltage drop across R2 is \( \approx \frac{R2}{R1} \) times greater than the Q8 emitter junction voltage drop; this relationship is used to fix the quiescent Q9, Q10 emitter voltage (approximately).

To the extent that this amplifier section approximates an idealized opamp the transconductance (ratio of voltage across the load to the current from the input stage) is \( \approx -R2 \). The current from the input stage is (approximately) \( (\beta/rbe)(v_+ - v_-) \), where rbe is the incremental base resistance of an (either) input transistor.

The differential input stage formed by Q4 and Q5 is drawn below. Q6 and Q7 form a current mirror to combine the two differential collector currents for input to the gain stage.