1) The Thevenin equivalent of a particular unregulated power supply is a voltage source $V_S$, where $10 \text{v} \leq V_S \leq 12 \text{volts}$, and an internal resistance $R_S = 50 \Omega$. Design a Zener diode shunt regulator (see circuit diagram) to provide a regulated 5 volt (nominal) output for $1 \text{K} \Omega \leq R_L \leq 2.5 \text{K} \Omega$. Use a 1N5231 Zener diode with a Zener voltage of 5.1 volts @ 20 mA, and nominal 10 Ω Zener resistance over the load current range.

**Answer**  Assuming regulation is active the load current will vary between $5.1/1 = 5.1\text{ma}$, and $5.1/2.5 = 2.04\text{ma}$. Estimate a minimum 'keep-alive' Zener current of $20/10 = 2\text{ma}$. This is the minimum current when the load current is a maximum, i.e., the source current must be at least $7.1\text{ma}$. Similarly the maximum Zener current is 20 mA, and this occurs for minimum load current. Hence the maximum supply current can be no more than 22 mA.

The 'worst case' condition for the minimum source current occurs with $V_S = 10 \text{v}$, and is $(10-5.1)/(R_S+R_B) \geq 7.1\text{ma}$. The 'worst case' condition for the maximum source current occurs with $V_S = 12 \text{v}$, and is $(12-5.1)/(R_S+R_B) \leq 22\text{ma}$. These inequalities require $313.6 \Omega \leq R_S+R_B \leq 690 \Omega$, and the specification of $R_S = 50 \Omega$ then requires $263.4 \leq R_B \leq 640 \Omega$. A nominal trial value of 470 Ω was selected.

A netlist for and a plot of a PSpice computation follows. Note the voltage scale of the plot.
*Problem 1 Linear Regulators

```
VS 1 0 DC {VVAL}   .LIB EVAL.LIB
RS 1 2 50
RB2 3 470
DZ0 3 D1N5231
IL 3 0 DC 20M
.MODEL D1N5231 D(Is=1.004f Rs=.5875
+ Ikf=0 N=1 Xti=3 Eg=1.11 Cjo=160p
+ M=.5484 Vj=.75 Fc=.5 Isr=1.8n Nr=2
+ Bv=5.1 Ibv=27.721m Nbv=1.1779
+ Ibvl=1.1646m Nbv=21.894 Tbv1=176.47u)
.PARAM VVAL = 10
.STEP PARAM VVAL LIST 10 12
.DC   IL 0M 15M .1M
.PROBE
.OP
.END
```

![Plot of PSpice simulation](image)
2) In problem 1 the regulating action of your design assumes the Zener diode operates in the breakdown region. For a large enough load current the diode current is insufficient to maintain breakdown. Estimate this dropout current for your design, and compare with a PSPICE analysis.

**Answer**  The design makes \( RS + RB = 520 \Omega \). Suppose \( VS = 12v \). Then the source current while the diode is in breakdown is \( \approx \frac{(12-5.1)}{0.52} = 13.27 \text{ ma} \). Therefore when the load current is (approximately) 13 ma the Zener diode will be starved for current.

Similarly anticipate dropout for \( VS = 10v \) at about 9ma.

3) Add a sinusoidal voltage source in series with \( VS \) (1.5 volt amplitude, 120Hz) to simulate a substantial rectifier ripple voltage. Estimate the ripple across the load assuming a nominal 10\( \Omega \) Zener resistance and a 1 K\( \Omega \) load resistance. Use PSPICE to obtain the load voltage transient response and compare to your estimate.

**Answer**  Approximate the Zener diode (in breakdown) as a 10\( \Omega \) resistor in series with a 5.1 v source. Apply superposition to relate the sinusoidal part of the output voltage to the sinusoidal input voltage;

\[
\text{Output 'ripple' } \approx 1.5 \frac{520}{520 + 10 + 1000} \]

\[
= 28 \text{ mv peak}
\]
4) The shunt regulator circuit discussed before is reproduced here for convenience (except that the load is shown as a DC current source). Given $V_S = 15$ volt, $R_S = 1\, \text{K}\Omega$. Select element values ($R_{B1}, R_{B2}$) to provide a nominal load voltage = 6.5 VDC for load currents from 0 to about 10mA. Compare the designed regulation performance with that of a PSPICE computation.

**Answer**

Estimate the source current while regulated as $(15-6.5)/1 = 8.5\, \text{mA}$. Estimate the 'reference' voltage at node 3 as 1.4V. The voltage at node 2 is to be a nominal 6.5V. Neglect (the effective current amplification $\approx \beta^2$) the base current to Q3, i.e., assume $R_{B1}$ and $R_{B2}$ form a simple voltage divider. From this determine $R_{B1}/R_{B2} = 3.64$. Trial values used are $R_{B1}=3.9\, \text{K}, R_{B2} = 1.2\, \text{K}$. The ratio $R_{B1}/R_{B2} = 3.25$, and the current in the 'divider' is about $1.4/1.2 = 1.17\, \text{mA}$. The netlist includes a computation for $R_{B1} = 3.9\, \text{K}, 4.7\, \text{K},$ and $5.6\, \text{K}$.

Since the junction voltages will be nominally fixed even for small currents regulation should fail when the load current is a bit less than the source current less the divider current, i.e., about 7mA.

Output is plotted below. Also shown (for $R_{B1} = 4.7\, \text{K}\Omega$ only) is the source current. As regulation fails the load voltage drops, increasing the source current.
5) The accompanying (simplified) circuit diagram interprets the series-pass regulator as a feedback system. The (idealized) amplifier in the circuit below includes the transistor emitter junction in the feedback loop. Assuming a constant reference voltage the amplifier maintains a constant output voltage which is a multiple of the reference voltage (but not so large as to saturate the pass transistor, or the amplifier).

Use a 741 opamp, a 2N3904 transistor, assume \( V_{\text{unreg}} = 25 \) volts, and a reference voltage of 2v. For a 10K\( \Omega \) potentiometer evaluate the (idealized) regulator performance.

**Answer** The idealized amplifier voltage gain is

\[
\frac{V_L}{V_{\text{ref}}} = \frac{RS_1 + RS_2}{RS_2}
\]

and for \( RS_1/RS_2 = 4,3,1,0.25 \) respectively \( V_L = 10, 8, 4, 2.5v \) This is confirmed by a PSpice analysis, for which a netlist is shown.

```plaintext
VUN 1 0 SIN(25, 2,120)
Q1 1 4 6 Q2N3904
VX 6 5 SIN(0,1,120)
XAMP 2 3 7 0 4 UA741
VREF 2 0 DC 2
V+ 7 0 DC 15
IL 6 0 DC 20M
.PARAM WIPER= 0.4
RS1 5 3 {10K*(1-WIPER)}
RS2 3 0 {10K*WIPER}
.STEP PARAM WIPER LIST 0.2 0.25 0.5 0.8
.TRAN 0.5M 20M
.LIB EVAL.LIB
.PROBE
.END
```

**Problem 5**

NOTE: For illustrative purposes the unregulated voltage has 'ripple' added, and a 'perturbation' VX is inserted.
A regulator design based on the feedback configuration discussed above is drawn below. A PSPICE netlist for the circuit is to the right. Identify the several subsystems of the regulator, and compute the circuit regulation behavior, i.e., the line regulation (load voltage vs $V_{\text{unreg}}$ at a fixed load current) and the load regulation (load voltage vs load current for a fixed $V_{\text{unreg}}$).

![Circuit Diagram]

*Problem 6

VUN 1 0 DC 25
RUN 1 2 250
RZ 2 3 4.7K
DZ 0 3 D1N5231
RF1 3 4 10K
RF2 4 0 10K
CF 4 0 4.7U
X1 4 5 9 10 11 UA741
V+ 9 0 DC 12
V- 10 0 DC -12
RXX 11 6 10K
Q1 2 6 7 Q2N3904
RE1 7 8 47
Q2 6 7 8 Q2N3904
RS2 5 0 [(WIPER)*10K]
RS1 8 5 [(1-WIPER)*10K]
IL 8 0 DC 10M
.MODEL D1N5231 D(Is=1.004f Rs=.5875 + Ikf=0 N=1 Xti=3 Eg=1.11 Cjo=160p + M=.5484 Vj=.75 Fc=.5 Isr=1.8m Nr=2 +Bv=5.1 lbv=27.721m Nbv=1.1779 + lbv=1.1646m Nbvl=21.894 Tbvl=176.47u)
.LIB EVAL.LIB
.PARAM WIPER = .4
.STEP PARAM WIPER .1 .5 .1
.DC IL 0m 15m .1m ;load regulation @ 25v
* DC VUN 0 15 .5 ;line regulation @ 10m
.PROBE
.END

**Answer**

Line regulation curves (output voltage vs. input voltage) are plotted below. For regulation to be initiated with a 10mA load current there will be (approximately) a 2.5 volt drop across the 250Ω 'internal resistance' of the unregulated source, approximately 0.5 volt drop across the transistor (to bring it out of saturation), and a 0.47 volt drop across the cutoff resistor. For an output voltage of, say, 8 volts (WIPER = 0.3) the unregulated input voltage will be about $2.5 + 0.5 + 0.47 + 8 = 11.47$ when regulation begins. This estimate can be compared with the appropriate computed line regulation characteristic. Note that the output voltages called out by WIPER = 0.1 and 0.2 cannot be supported because the amplifier saturates in both case.
Computed load regulation curves are plotted next. The cutoff current is estimated as $0.6/47 \approx 13$ ma.

7) Reanalyse the regulator of problem 6 using a resistive load $RL$ in place of the current source $IL$. To obtain a plot with resistance as the independent variable:

Define $RL$ with $RL \ N+ \ N- RMOD \ 1$, and define $RMOD$ by $>MODEL RMOD RES$. Then to sweep use $DC \ RES \ RMOD(R)$ start end increment.

The sweep values actually are multipliers of the value assigned to $RL$, but since the value 1 was assigned they are equal to the resistance values.

<table>
<thead>
<tr>
<th>*Problem 7</th>
<th>Answer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VUN</strong> 1 0 DC 25</td>
<td>RS2 5 0 {WIPER*10K}</td>
</tr>
<tr>
<td><strong>RUN</strong> 1 2 250</td>
<td>RS1 8 5 {(1-WIPER)*10K}</td>
</tr>
<tr>
<td><strong>RZ</strong> 2 3 4.7K</td>
<td>RL 8 0 RMOD 1</td>
</tr>
<tr>
<td><strong>DZ</strong> 0 3 D1N5231</td>
<td>.MODEL RMOD RES</td>
</tr>
<tr>
<td><strong>RF1</strong> 3 4 10K</td>
<td>.MODEL D1N5231 D(Is=1.004f Rs=.5875</td>
</tr>
<tr>
<td><strong>RF2</strong> 4 0 10K</td>
<td>+ Ikf=0 N=1 Xti=3 Eg=1.11 Cjo=160p</td>
</tr>
<tr>
<td><strong>CF</strong> 4 0 4.7U</td>
<td>+ M=.5484 Vj=.75 Fc=.5 Isr=1.8n Nr=2</td>
</tr>
<tr>
<td><strong>X1</strong> 4 5 9 10 11 UA741</td>
<td>RF1 3 4 10K</td>
</tr>
<tr>
<td><strong>V+</strong> 9 0 DC 12</td>
<td>RF2 4 0 10K</td>
</tr>
<tr>
<td><strong>V-</strong> 10 0 DC -12</td>
<td>CF 4 0 4.7U</td>
</tr>
<tr>
<td><strong>RXX</strong> 11 6 10K</td>
<td>+ Rb=5.1 Ib=27.721m Nb=21.894 Tb=176.47u</td>
</tr>
<tr>
<td><strong>Q1</strong> 2 6 7 Q2N3904</td>
<td>x1 4 5 9 10 11 UA741</td>
</tr>
<tr>
<td><strong>RE1</strong> 7 8 47</td>
<td>.LIB EVAL.LIB</td>
</tr>
<tr>
<td><strong>Q2</strong> 6 7 8 Q2N3904</td>
<td>.PARAM WIPER = .4</td>
</tr>
</tbody>
</table>

**.STEP PARAM WIPER .1 .5 .1**

**.DC RES RMOD(R) 20K .1K .1K**

**.PROBE**

**.END**
This next plot simply presents the data in a different fashion. Since the load voltage $V(8)$ is $R \times I(RL)$ then to the extent the output voltage is regulated a plot of $1/I(RL)$ vs $R$ will be a line whose (constant) slope is $1/V(8)$.

A principal concern for series regulators is the power dissipated in the pass transistor; 'hard' current limiting to prevent excessive current was described earlier. However limiting sets in for approximately the same current at all regulated load voltages. But the voltage across the pass transistor is a maximum for minimum load voltage, and so a higher rated load current for a given power handling capability could be permitted for larger load voltages. The circuit to the right shows a modified limiting circuit which accomplishes this.

While the base is biased to a voltage less than the load voltage $VL$ the emitter junction voltage $V_{BE}$ of the (cutoff) current-limiting transistor is
The voltage divider ratio $k$ determines the relative influence of the load current and voltage in current limiting. Note that for a given load current $V_{BE}$ is smaller the larger the load voltage, i.e., a larger load current is needed to reach a given threshold. This expression should not be used to relate the load voltage to the load current. Rather $V_{BE}$ should be set to the (fixed) transistor threshold voltage $V_{BE0}$, and the equation used to describe the locus of $(VL, IL)$ coordinates for which the threshold is reached.

Regulation curves appear generally as indicated; the cutoff line is superimposed. $V_{BE0}$ is the threshold junction voltage ($\approx 0.6$V), and the current intercept on the abscissa is $V_{BE0}/kR$.

The simplified series regulator circuit drawn to the right has been modified to apply 'foldback' current limiting. Compute and evaluate the foldback characteristics; compare to estimated behavior.

**Answer**

A PSpice netlist for circuit computations is to the right. For the circuit shown $k = 18/(6.8+18) = 0.73$, and $R$ is 220$\Omega$. Hence the 'fold-over' line is estimated to be $1.68M*VL + 3.74M$.

Computations are made varying the load voltage $VL$; the load current $I(VL)$ is then plotted. The computations for the several sampling ratios shown, together with the estimated fold-over line.

Note: It is convenient to use a voltage source as a load partly because the characteristic is a single-valued function of the load voltage.

```
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Computations are made varying the load voltage $VL$; the load current $I(VL)$ is then plotted. The computations for the several sampling ratios shown, together with the estimated fold-over line.

Note: It is convenient to use a voltage source as a load partly because the characteristic is a single-valued function of the load voltage.

Problem 8
VUN 8 0 DC 20
RUN 8 7 50
RB7 4 56K
X1 1 2 10 0 3 UA741
RX1 3 4 10K
Q1 7 4 6 Q2N3904
VREF 1 0 DC 2
V+10 0 DC 15
RCL 6 9 220
R1 6 5 6.8K
R2 5 0 18K
Q2 4 5 9 Q2N3904
VL 9 0 DC 1
.DC VL 0 10 0.1
.PARAM WIPER= 0.4
RS1 9 2 \{50K*(1-WIPER)\}
RS2 2 0 \{50K*WIPER\}
.STEP PARAM WIPER LIST 0.25 0.4 0.5 + 0.6 0.7
.LIB EVAL.LIB
.PROBE
.END
```
Design a series-pass regulator to provide a nominal -5 volts load voltage from a -15 volt unregulated supply.

**Answer** The essential circuit considerations are not changed because the unregulated voltage is negative. Details are illustrated in the circuit diagram. Indeed only the NPN transistor from the previous diagram is changed to PNP to accommodate the current flow. (Also the opamp supplies; the previous example operated on a single rail.)
10) For some purposes a current regulator is useful; the circuit diagram drawn to the right is a simplified current regulator. While the amplifier is active (not saturated) it adjusts the transistor emitter current so as to maintain a near-zero amplifier input voltage, i.e., $\text{Vref} - 0.47 \times I_L = 0$.

As $RL$ is decreased the voltage at node 4 decreases (assuming constant current) and consequently $V(3)$, and the amplifier output voltage also, must decrease. Eventually this voltage becomes less than $\text{Vref}$, the minimum value required to maintain the current, and $Q1$ then rapidly cuts off.

Conversely, as $RL$ is increased, $V(3)$ rises, pulled up by the amplifier output. Eventually the amplifier saturates, $V(3)$ sticks at about $Vsat - 0.7$, and the load current decreases as $RL$ increases ($\sim 1/RL$).

A PSPICE analysis of the circuit illustrates the circuit operation, as in the following plot. For a 741 opamp operating with ±12 volts supplies $Vsat \approx 12 - 0.7 = 11.3$ v. The voltage across $RL+470$ is estimated by subtracting the $Q1$ junction voltage drop; this is 10.6 v, and $10.6/(470+RL)$ is the estimated current at which regulation fails.

Perform a PSPICE analysis to confirm and extend the remarks made.