Differential Amplifier Problems

1) Calculate the voltage gain $V_o/V_i$ at a nominal frequency of 1 KHz, and compare to the computed value. Note that the single-ended source is electrically equivalent to applying the double-sided differential mode signals $V_i/2$ and $-V_i/2$. Also Q1 and Q2 are 2N3904.

Calculate the Q3 emitter current; assume this divides equally between Q1 and Q2.

$$I_E^3 = \frac{10 \left( \frac{22}{22+68} \right) - 0.7}{1 + \frac{22||68}{121}} = 1.53 \text{mA}$$

Estimate $r_{be}$ (each device) as $(2/1.53)(121)(26) \approx 4.1 \text{K}$. The incremental parameter equivalent circuit is as shown:

Note that the effective difference voltage magnitude is $V_i/2$. Calculate the gain magnitude as

$$G^V = \left| \frac{V_a - V_b}{0.5 - (-0.5)} \right|$$

$$= \left| \frac{1}{1+4.1} \left( -120 \right)(2.2) \right|$$

$$= 51.76 \text{ (34.3 dB)}$$

A PSpice netlist for the circuit follows:

* Problem 1

```
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VI 1 0 AC 1
RB1 1 2 1K
Q1 3 2 4 Q2N3904
RC1 5 3 2.2K
Q2 6 7 4 Q2N3904
RC2 5 6 2.2K
RB2 7 0 1K
Q3 4 8 9 Q2N3904
R3A 8 0 68K
R3B 8 10 22K
RE3 9 10 1K
VCC 5 0 DC 10
VEE 10 0 DC -10
.OP
.LIB EVAL.LIB
.AC LIN 1 1K 1K
.PRINT AC Vdb(6) Vdb(3)
.END
```
2) The signal source for the amplifier circuit of Problem 1) is changed to two sinusoidal sources as described in the accompanying netlist. Two transient computations are performed, one for differential-mode signals and the other for common-mode signals. Measure the output between the Q1-Q2 collectors.

Problem 2

```
VIN1 1 0 SIN(0 0.02 1K 0 0) R3B 8 10 22K
RB1 1 2 1K RE3 9 10 1K
Q1 3 2 4 Q2N3904 VCC 5 0 DC 10
RC1 5 3 2.2K VEE 10 0 DC -10
Q2 6 7 4 Q2N3904 OP
RC2 5 6 2.2K PROBE
RB2 7 12 1K LIB EVALLIB
VIN2 12 0 SIN(0 {AMPL} 1K 0 0) OP
.PARAM AMPL=1M .STEP PARAM AMPL LIST -0.02 0.02
Q3 4 8 9 Q2N3904 END
R3A 8 0 68K
```

![Graph showing differential and common mode signals](image-url)
3) Estimate the incremental transconductance gain neglecting Early Effect. Compare the estimate with the computed value.

*Problem 3

VIN 1 0 DC 0
RB1 1 2 1K
Q1 6 2 3 Q2N3906
RE 4 3 2.2K
Q2 7 5 3 Q2N3906
RB2 5 0 1K
Q3 4 6 8 Q2N3904
Q4 6 8 9 Q2N3904
Q5 7 8 9 Q2N3904
RL 7 0 100
VCC 4 0 DC 10
VEE 9 0 DC -10
.LIB EVAL.LIB
.DC VIN -.2 .2 10M
.OP
.PROBE
.END

![Graph showing the relationship between input voltage (VIN) and output current (I(rl))](image)

![Graph showing the relationship between input voltage (VIN) and output current (I(Q2), I(Q5))](image)
4) **Amplitude Modulator Illustration**

The differential amplifier circuit is used to form an efficient amplitude modulator (Gilbert Cell). The simplified circuit diagram shown is used to illustrate the general character of the modulation process. The single-ended carrier sinusoidal signal VC is used to switch Q3 and Q4 alternately between cutoff and an amplifying state in which the bias current is provided by Q5. That bias current, and so the differential gain of the amplifier, is varied sinusoidally by the modulating signal VM. The differential output then is proportional to a product of the two sinusoids, i.e., a sinusoid whose amplitude varies sinusoidally. A small resistance is added in the Q2 emitter path to offset the Early Effect.

In the example that follows the modulating sinusoidal signal has a 3v amplitude and a frequency of 1KHz. The carrier, a sinusoid with a 5v amplitude, has a frequency of 20 kHz. The higher frequency product signal can be transmitted as a radio wave more efficiently than the modulating signal itself; the modulation can be recovered by a rectification and filtering process. (In practice the carrier should have a much higher frequency than the modulating signal; the choice made for this illustration shows the basic modulation effect, and provides relative computational simplicity.)

```
* modulator

VC  1 0 SIN(0 5 20K)
RB1  1 2  1K
Q3  3 2  7 Q2N3904
Q1  3 3  4 Q2N3906
Q2  5 3 12 Q2N3906
RX  4 12  1.2
Q4  5 6  7 Q2N3904
RB2  6 0  1K
RL  5 0  100
Q5  7 8 10 Q2N3904
RA  8 9  47K
RB  8 11  10K
VM  9 0  SIN(0 3 1K)
RE  10 11  100
VCC 4 0 DC  10
VEE 11 0 DC -10
.LIB EVAL.LIB
.PROBE
.TRAN 10U 2M
.END
```

![Circuit Diagram](Image)