1. Consider the given circuit with $\beta = \beta_0 = 100$, $V_{CC}$ is 15V, and $-V_{CC}$ ($V_{EE}$) is -10.7V.

   a) (5) What is the voltage gain of the circuit if $V_1=V_2$ given that $R_2 = R_3 = 20K$ and $R_1 = 40K$?
   
   b) (5) What is the input impedance of the circuit if $V_1=-V_2$?
   
   c) What is $V_{CEO}$?
   
   d) (5) How does the CMRR of the circuit vary as $V_{CC}$ is varied?
   
   e) (5) Suppose $V_1$ and $V_2$ have a DC offset +.7V DC. What is $V_{CEO}$ now?
2. You are to design a 9 W Class B public address amplifier with one input that will operate off of a pair of batteries of equal voltages and provide a voltage gain of 100. Assume that available op amps have a gain-bandwidth product of 1 MHz and can come within .3V of the rail voltage. An 8-ohm speaker will be used.

a) (5) If the upper frequency limit of the amplifier is to be 25 kHz, how many op amps will you need to provide the necessary bandwidth?

b) (5) Draw your circuit showing component values and biasing including quiescent voltage values minimizing component count and cost. The low-frequency cutoff is to be 50 Hz. (Hint: use only a single capacitor!)

c) (5) What is the minimum value of the battery voltages that still meets the power requirement?

d) (5) Given that class B amplifiers have distortion, explain how your circuit minimizes the problem. Class AB operation is not an option here.

e) (5) What input signal is required to drive the amplifier to full power?
3. You are to design a common-collector amplifier with $I_{CQ} = 20\,mA$ with a 15.7V supply that will drive a 100 Ohm load. Operation will be in class A mode and an op amp is to be used with global feedback so that the overall voltage gain is -9.

a) (5) Design the current source and calculate necessary component values.

b) (5) Design the amplifier circuit such that the low-frequency cutoff is 50 Hz. Do not allow any bias currents to flow in either the input signal source or the

c) (5) What is the input impedance of the amplifier?

d) (5) What is the maximum undistorted power output?

e) (5) What is the high-frequency cutoff of the amplifier assuming that the op amp has a 1MHz gain-bandwidth product?
4. (5) Draw a three-input CMOS OR gate.

5. (5) Why are NAND gates preferred over NOR gates for CMOS logic?

6. (5) When building high-gain or high-bandwidth amplifier circuits, the use of __________________________ across the rails can significantly improve stability.

7. (5) With a given supply voltage and load, a bridge amplifier can increase the power by a factor of ______ compared to a single (unbalanced) amplifier.

8. (5) When using a bridge amplifier, damage to the output transistors may occur because the load current is increased by a factor of ______ compared to a single (unbalanced) amplifier.

8. (5) Describe one way to prevent thermal runaway in a class AB amplifier when using diodes for biasing.