1. Consider the given circuit with $\beta = \beta_0 = 100$, $V_{CC}$ is 15V, and $-V_{CC} \ (V_{EE})$ is -10.7V.

a) (10) What is the voltage gain of the circuit if $V_1=V_2$ given that $R_2 = R_3 = 5K$ and $R_1 = 5K$?

b) (10) What is the output impedance of this amplifier?

c) (10) How does the CMRR of the circuit vary as $-V_{CC} \ (V_{EE})$ is varied?

d) (10) Draw a circuit specifying necessary values to increase the CMRR by about 20 dB.

e) (10) Given that $V_1=-V_2$, how would you modify the circuit so that the input impedance was 500K??
2. You are to design a 25 W Class B public address amplifier with one input that will operate off of a pair of batteries of equal voltages and provide a voltage gain of 100. Assume that available op amps have a gain-bandwidth product of 1 MHz and can come within .3V of the rail voltage. A 4-ohm speaker will be used.

a) (10) If the upper frequency limit of the amplifier is to be 20 kHz, how many op amps will be needed to provide the necessary gain and bandwidth?

b) (10) Draw your circuit showing component values and biasing including quiescent voltage values minimizing component count. The frequency response is to go down to DC.

c) (10) What is the minimum value of the battery voltages that still meets the power requirement?

d) (10) What input signal is required to drive the amplifier to full power?

3. (10) Why are NAND gates preferred over NOR gates for CMOS logic?