Opamp Gain-Bandwidth

This illustration is taken from an old ECE311 problem set, and distributed as a tutorial exercise. You should make an effort to realize a design before examining the illustrative design on the next page.

The nominal Gain-Bandwidth product for the 741 OpAmp is 1MHz (80 db, 100 Hz), i.e. the expression for the gain at a frequency f is

$$\frac{10^4}{2\sqrt{1 + \left(\frac{f}{100}\right)^2}}$$

Suppose an amplifier is to be designed for a midband gain of 40 db, and a 3dB rolloff frequency of 100kHz. A not unexpected novice proposal would be to suggest either a non-inverting or an inverting configuration as illustrated, with an appropriate choice of resistor values.

Unfortunately with a gain of 40 db the 3 db bandwidth realized is only 10 kHz!

A two-stage (identical stages, for simplicity) cascade might be considered next, with a per-stage gain of 20db; the corresponding stage bandwidth is 100 kHz.

Unfortunately the cascade gain is down 6db at this frequency, a 3db reduction for each stage. The actual 3db frequency is 64.4 kHz.

Design a cascade of noninverting 741 amplifiers for a gain of at least 40db at 100 kHz. Describe the basis for design choices you make, so that it is clear that your design is not simply a lucky guess?

Note:
- A 'by guess and by golly' circuit uses four stages.
- A minimal design effort uses three stages.
- A degree of (advanced) sophistication and you can get by with just two stages.
Answer

This problem is intended to increase awareness of the Gain-Bandwidth constraint, generally applicable, but here specifically in the OpAmp case. The nominal Gain-Bandwidth product for the 741 OpAmp is 1MHz (80 db, 100 Hz). Suppose a single stage amplifier (inverting or noninverting) is proposed. Unfortunately with a gain of 40 db the bandwidth realized is only 10 kHz!

Use three identical stages, 14db per stage, to obtain a nominal 42db overall midband gain.

\[ \frac{5}{\sqrt{1 + \left( \frac{f}{199.5} \right)^2}}^3 \]

and this will be \( 125/\sqrt{2} \) when \( f = 101.7 \text{KHz} \).

The results for a PSpice computation are drawn below.

Introducing external poles and zeros in the transfer function appropriately also can extend the bandwidth of an amplifier. For a particular illustration suppose a small capacitor is added across the 220\( \Omega \) feedback resistor of each stage. Qualitatively this may be viewed as replacing the resistor by an impedance whose magnitude decreases as the frequency increases. This also decreases the feedback, and so the gain increases (i.e. is decreased less by the feedback). The effectiveness of this compensation depends on the gain of the amplifier without feedback being high enough to make feedback meaningful, and eventually at a high enough frequency this compensation will fail.

The singularity is set (ad hoc) at about the 200KHz pole of the inherent amplifier stage. The response for several values of capacitance is shown below. (For a 0.1 nF capacitance value the response is essentially that absent the capacitor.) Note particularly the response for a 1 nF capacitor.
The three-stage design modification suggests that the 40 db-100 MHz bandwidth requirements just might be satisfied using just two stages. The 'pole-cancellation' procedure was applied (casually) to a two-stage amplifier design, with the frequency response computed by PSpice as shown below. Note in particular the 2 nF response.